

# X570 AORUS ELITE

PAGE	TITLE	Revision : 1.0
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	R_USB30_1	
18	F_USB30_1 , F_USB30_2	
19	IT8688E	
20	A_VDD1V8 / A_VDDPS5	
21	ALC1220-VB2 CODEC	
22	AUDIO JACK	
23	VCORE_SOC	
24	POWER SEQUENCE , A_VDDP	
25	PWM INTERSIL69147	
26	VCORE MOS	

PAGE	TITLE
27	VCORE MOS
28	VCORE_SOC MOS
29	VPP_MEM , NCT3933U
30	5VDUAL , 3VDUAL , VDDIO_MEM , DDRVTT
31	INTEL LAN WGI211AT
32	M2A_SOCKET
33	M2B_SOCKET , SATA3_4_5
34	N/A
35	PCIEX4 , PCIEX1_1 ,PCIEX1_2
36	CPU SMD CAP TOP , HEATSINK
37	CPU SMD CAP BOTTOM
38	N/A
39	F_USB31C , M2_WIFI
40	N/A
41	N/A
42	N/A
43	THB_C , TPM , H/W MONITOR
44	N/A
45	N/A
46	MCU IT8297
47	AUDIO LED
48	D_LED1 , D_LED2
49	FAN CONTROL
50	ATX , FRONT PANEL
51	HDMI
52	R_USB30_2
53	USB2.0 HUB GL850S , F_USB1 , F_USB2 , R_USB
54	REDRIVER PI3EQX1002B1ZLE
55	PM_1VSOC , PM_1V8 , PM_09SOCS5 , PM_CLDO12

2015.12.30~B.L

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Title

Size

Custom

Document Number

X570 AORUS ELITE

Date:

Monday, May 13, 2019

Rev

1.0

Sheet

1

of

55

COVER SHEET

**Model Name : X570 AORUS ELITE**

### Component value change history

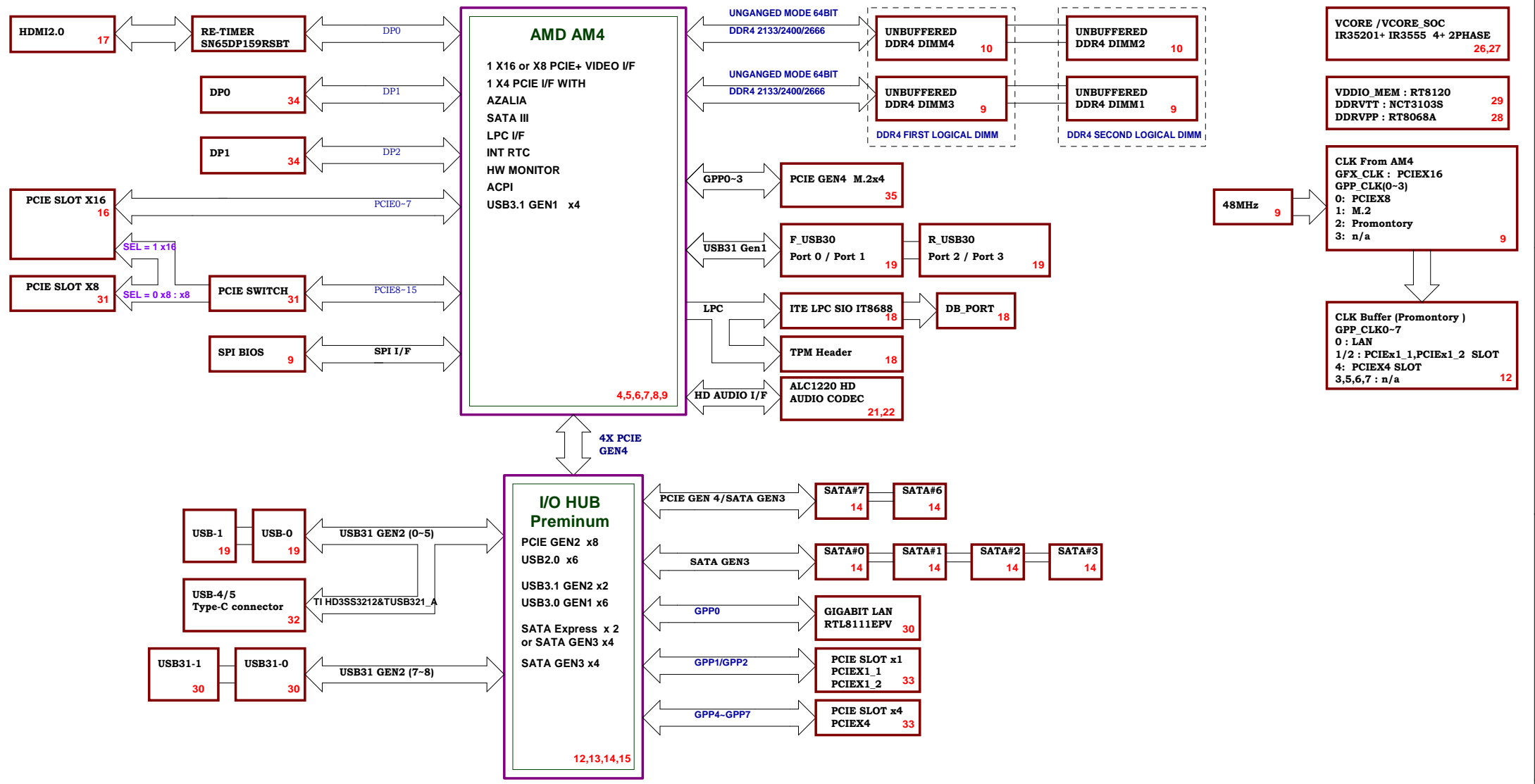
**Version: 1.0**

**P-Code: U98126-0**

[illegible]

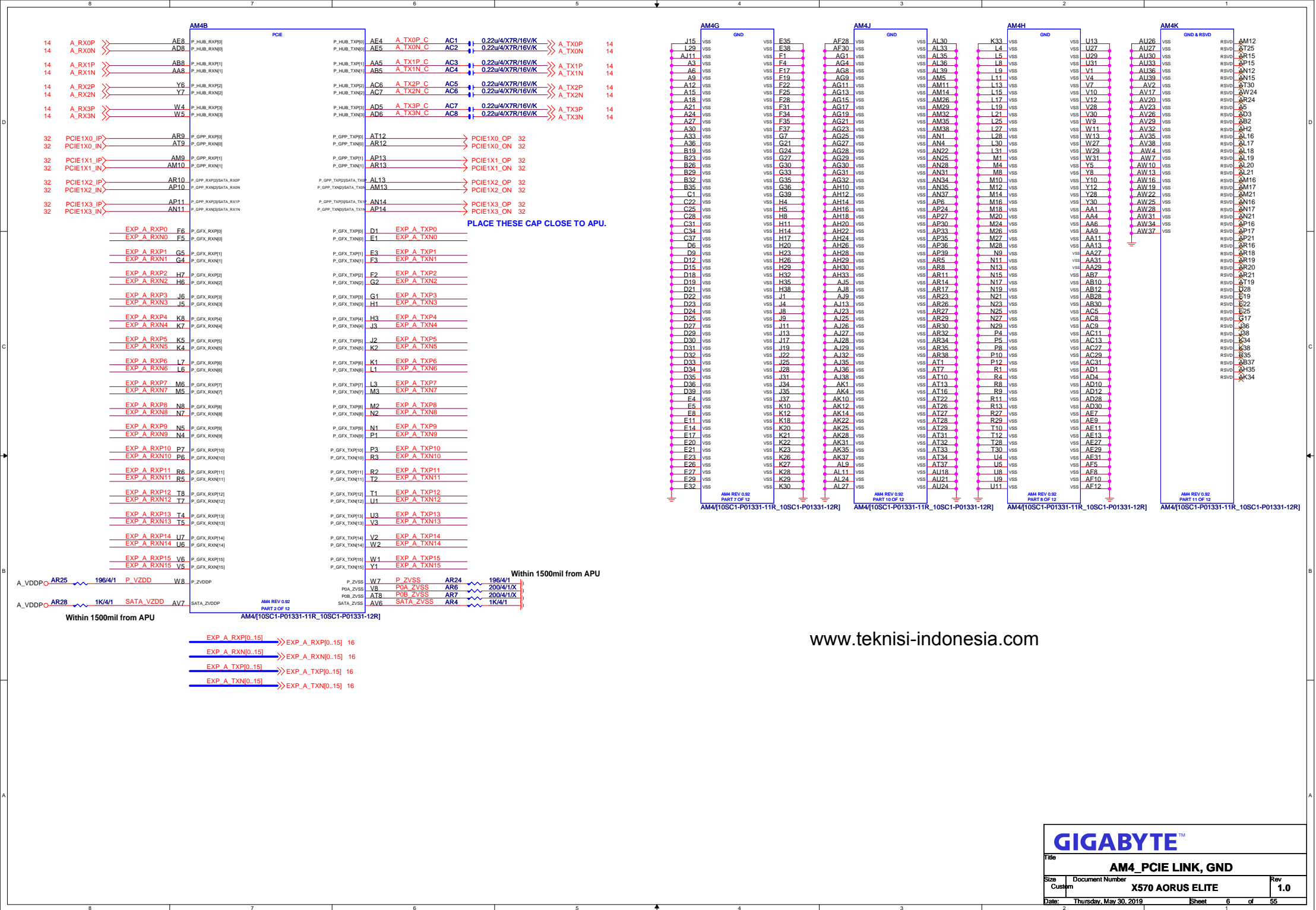
### Circuit or PCB layout change for next version

[illegible]



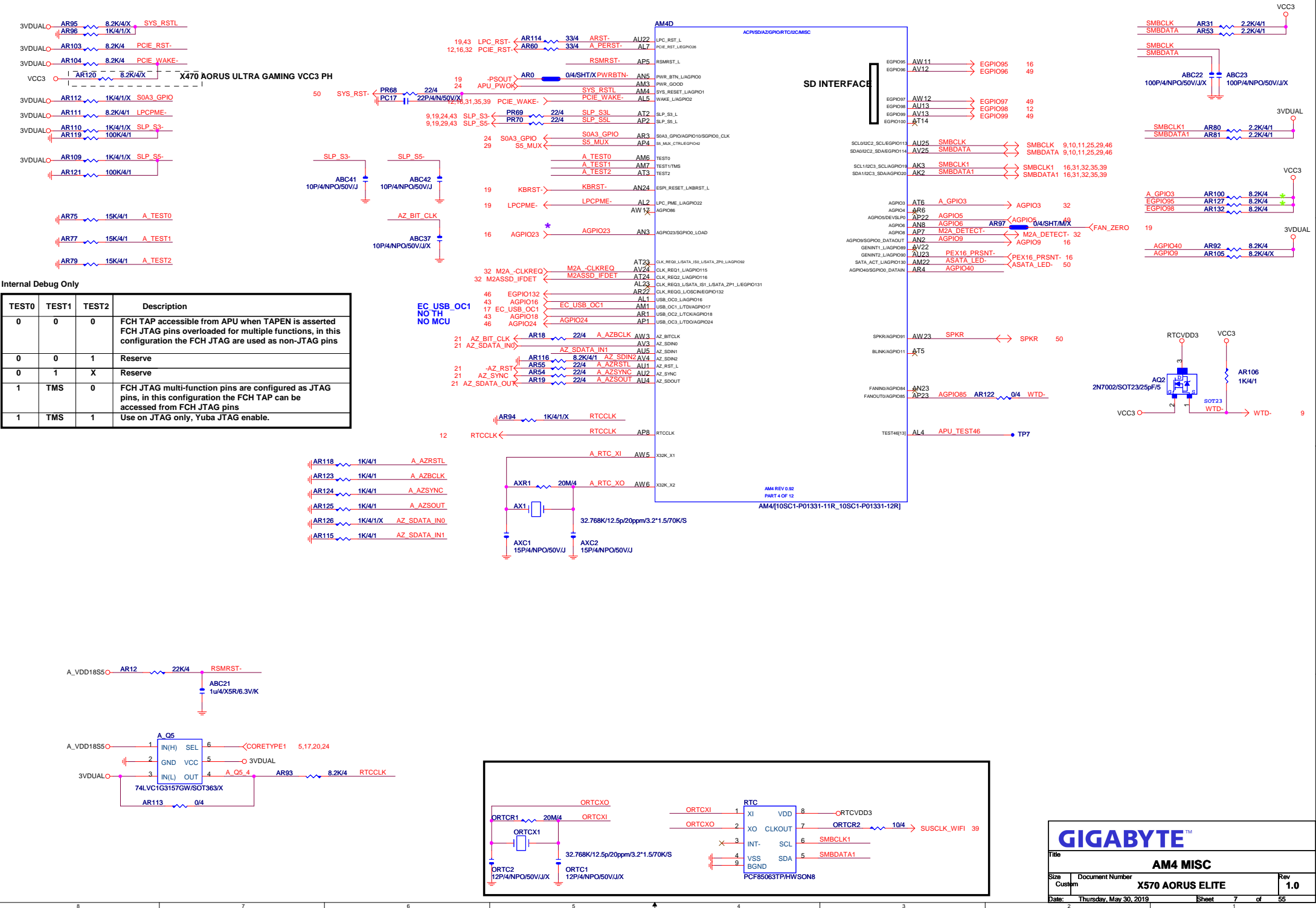




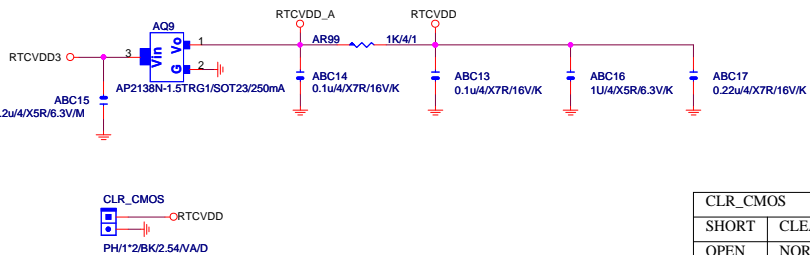
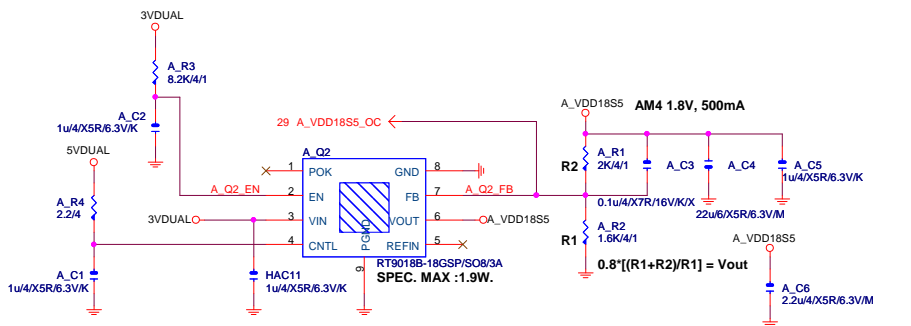
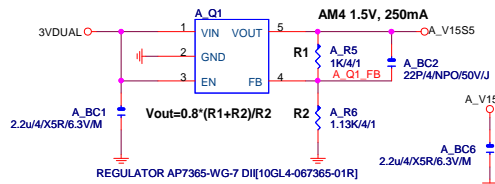
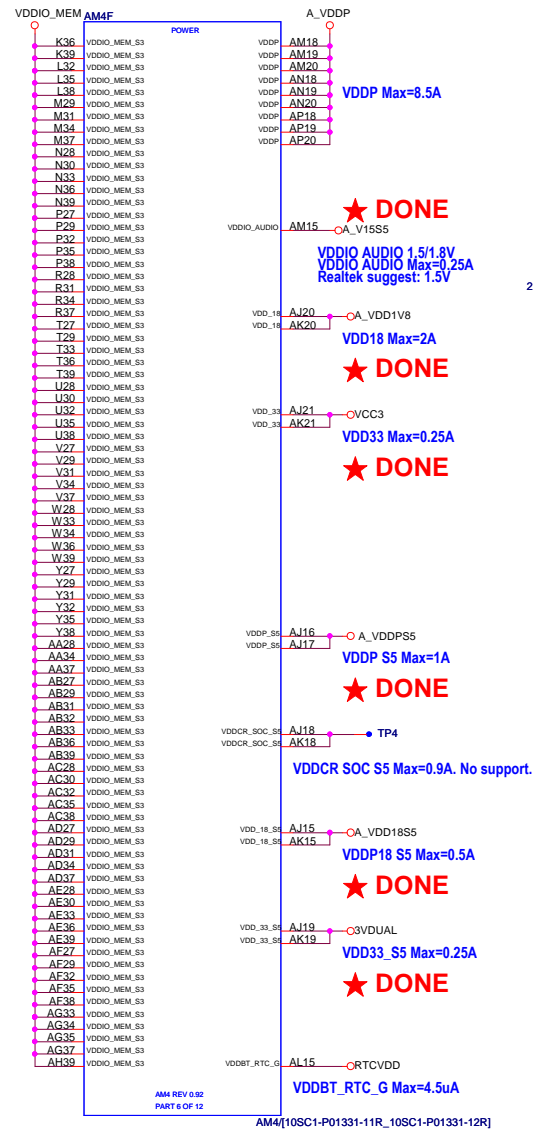


Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH JTAG can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

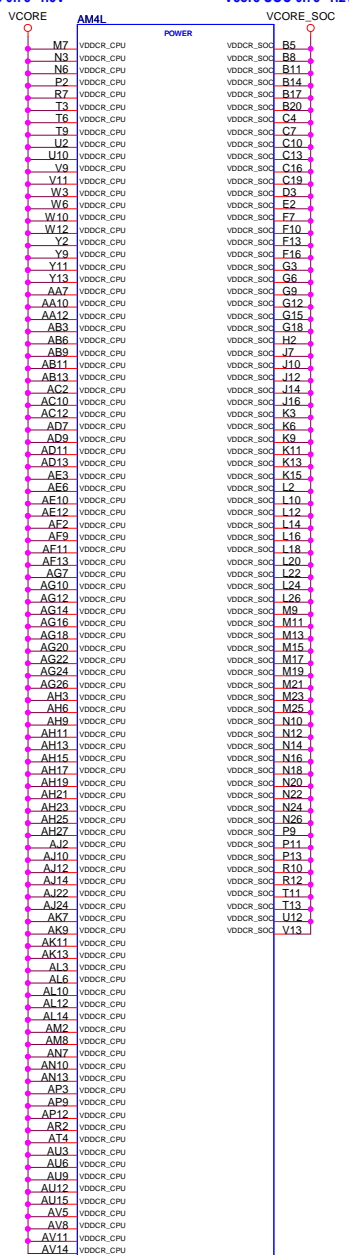


VDDIO Max=15.5A



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

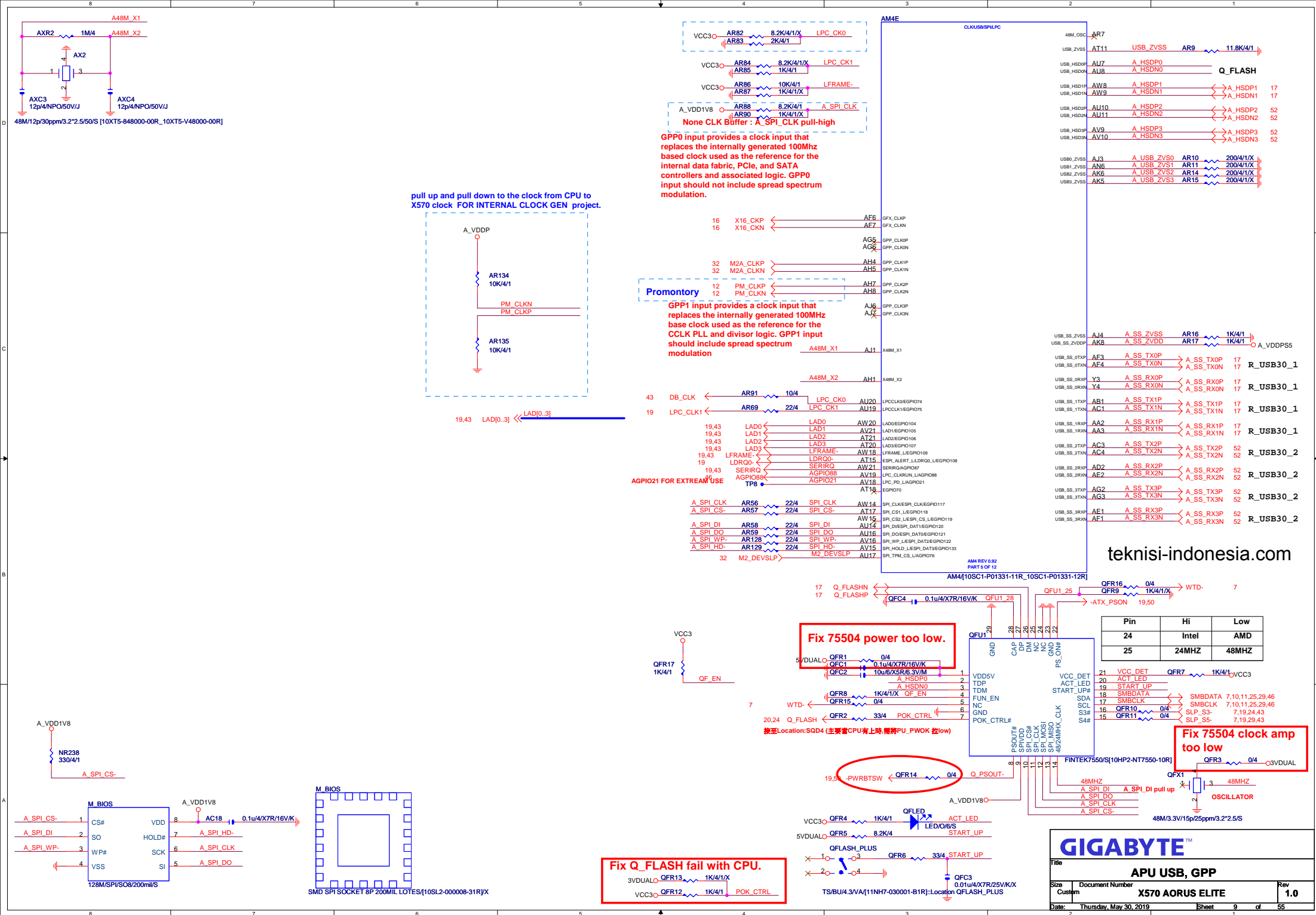
Vcore EDC=75A  
Vcore 0.75-1.5V

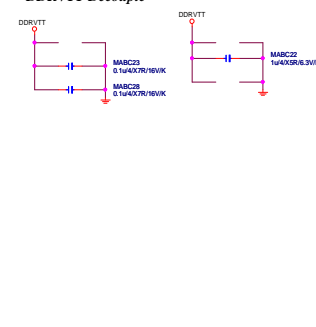
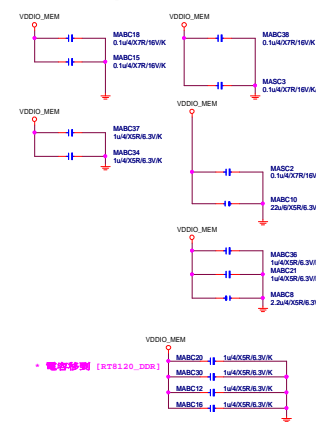
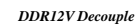
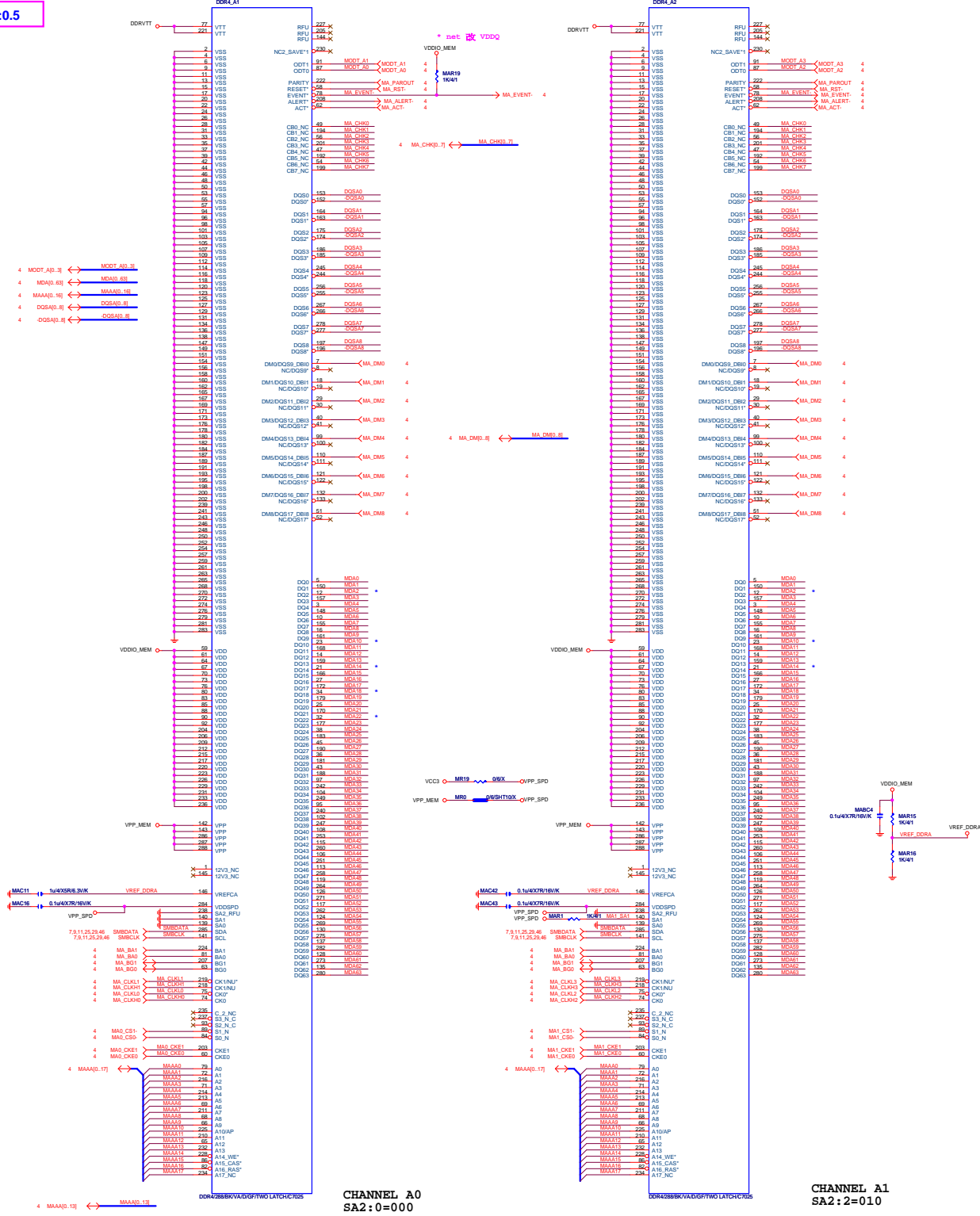


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CPU POWER & GND			
Size	Document Number	X570 AORUS ELITE	Rev 1.0
Date	Thursday, May 30, 2019	Sheet 8 of 55	

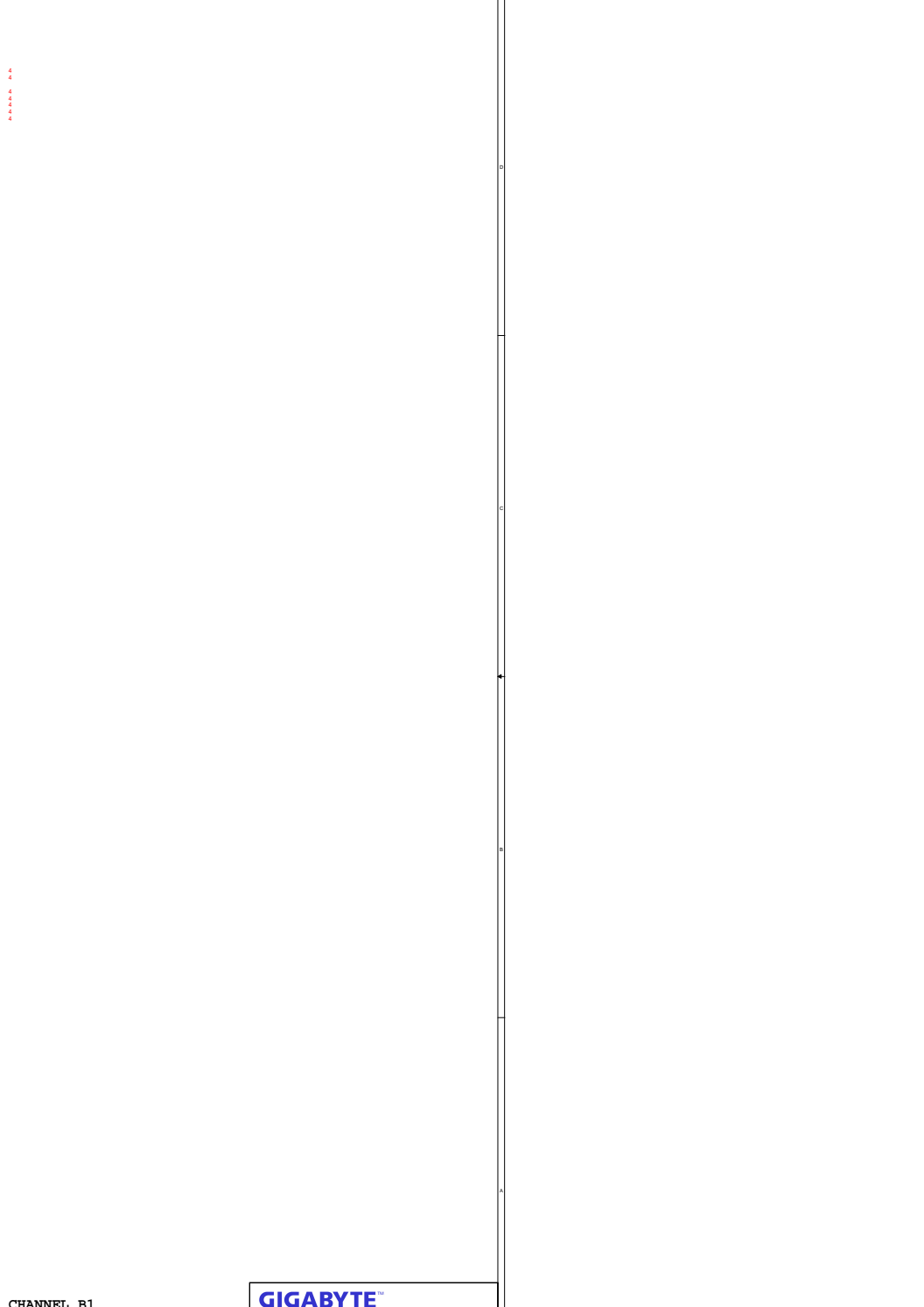




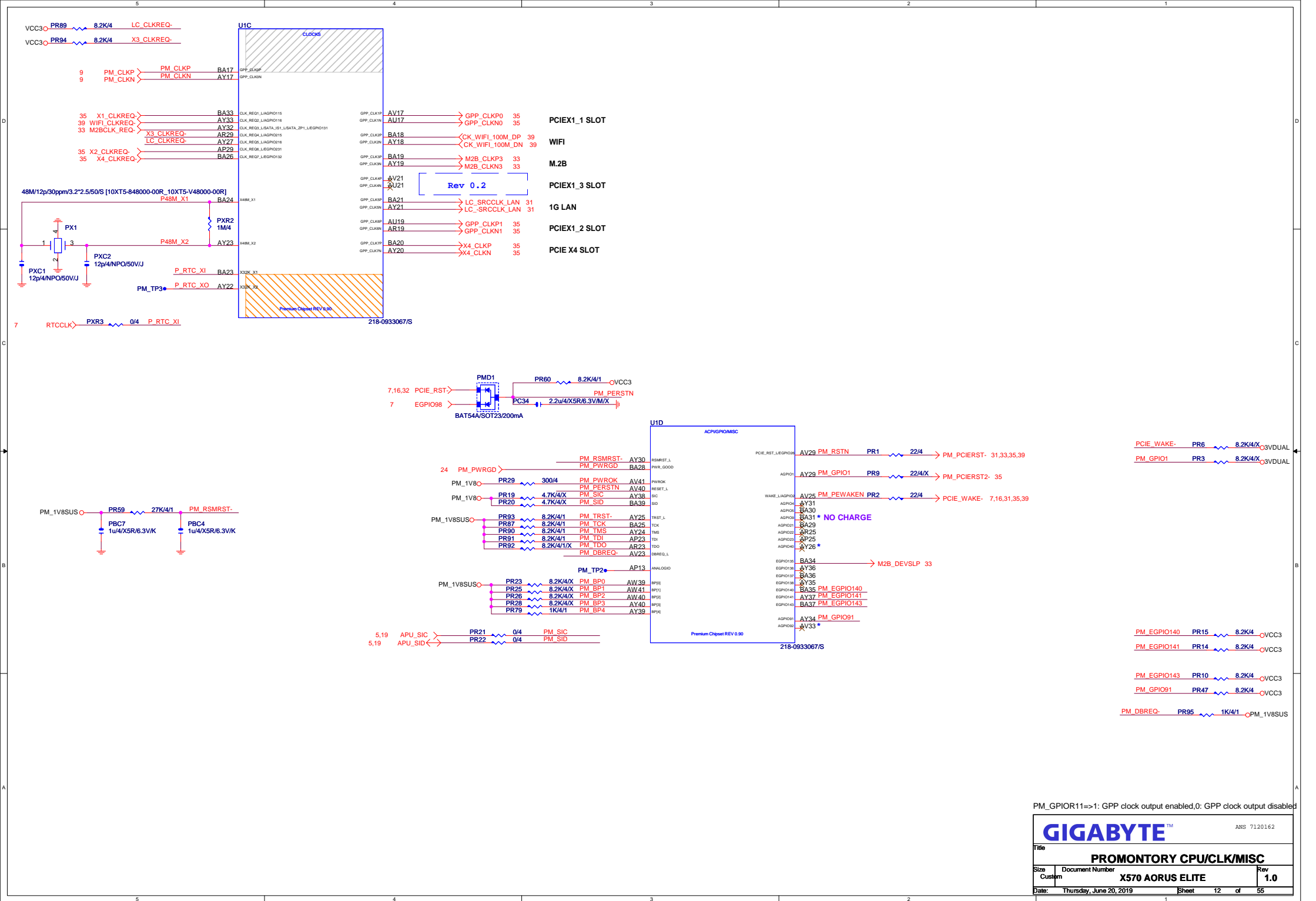


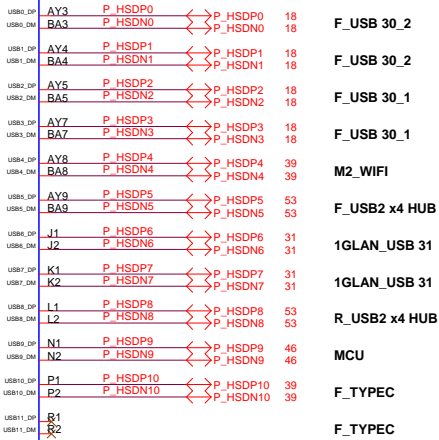
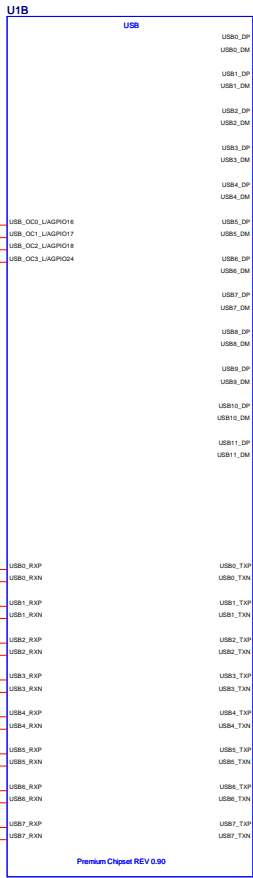


CHANNEL B0  
SA2:1=001

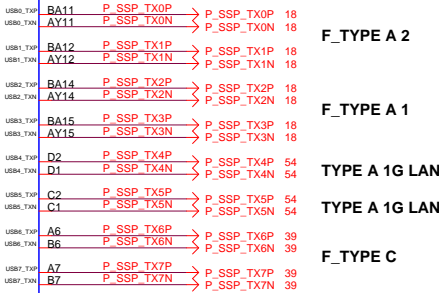
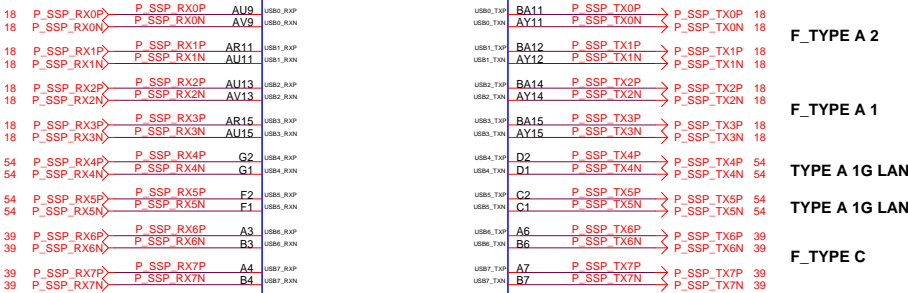


CHANNEL B1  
SA2:3=011





USB 3.1 Gen 2



USB Controller 0: USB20 [0:5], USB30 [0:3]

USB Controller 1: USB20 [6:11], USB30 [4:7]

USB Controller 0: USB20 [0:5], USB30 [0:3]

USB Controller 1: USB20 [6:11], USB30 [4:7]

USB30G2	USB20
0	0
1	1
2	2
3	3
4	6
5	7
6	10
7	11

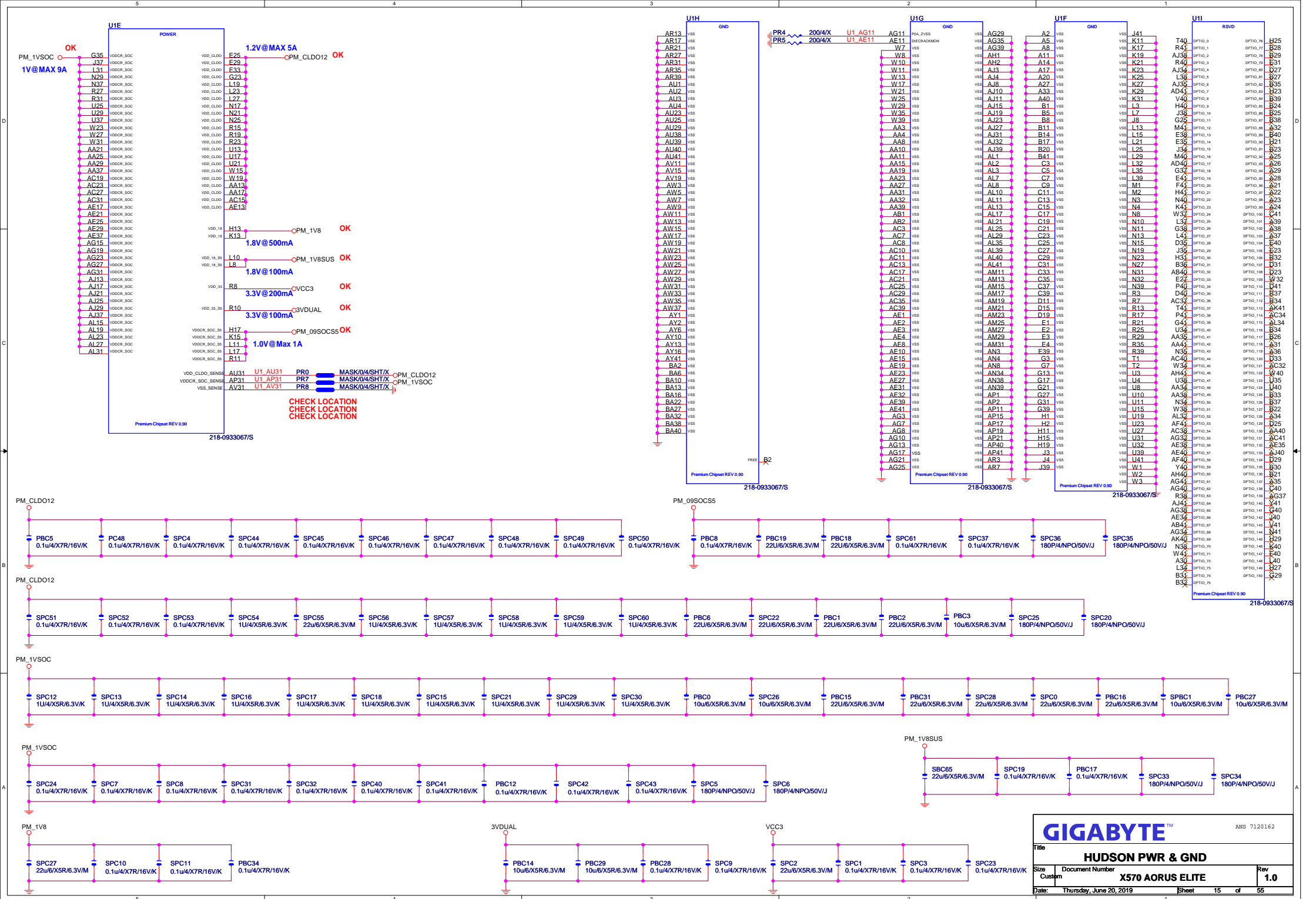
F\_USB 30\_2

F\_USB 30\_1

USB30\_I211 Lan

FRONT TYPE C



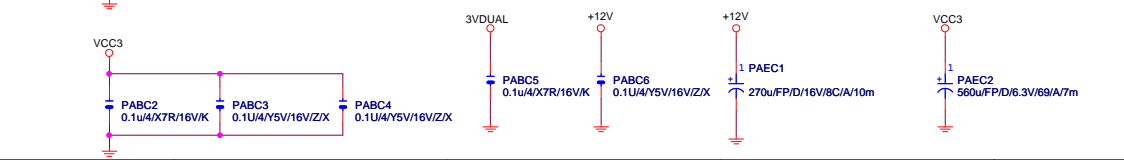
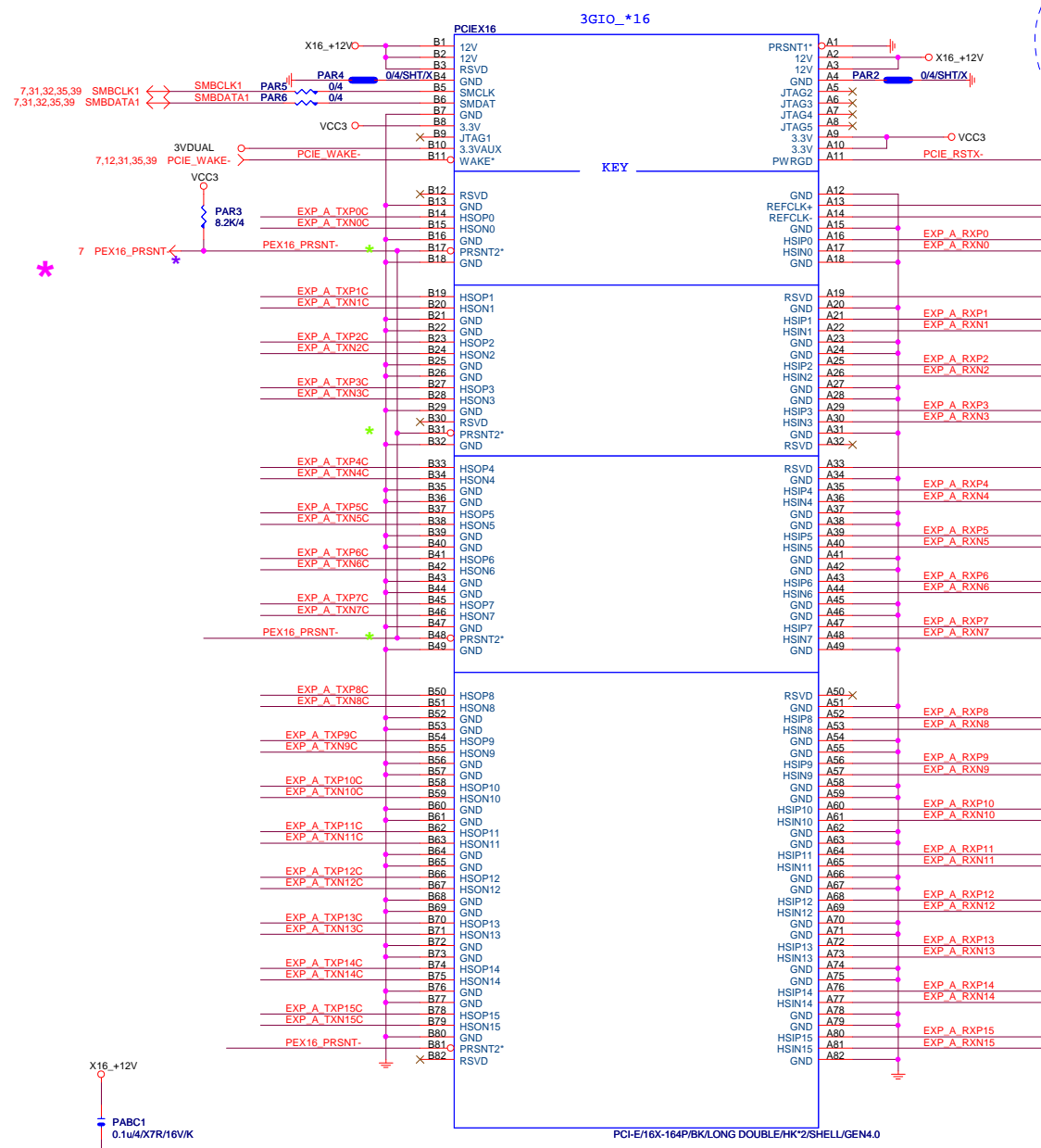
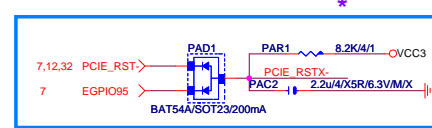


+12 - protect  
short-wire test

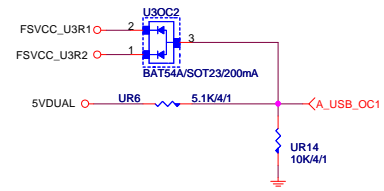
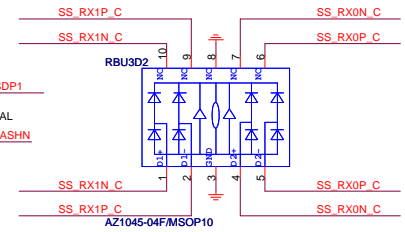
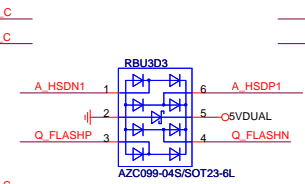
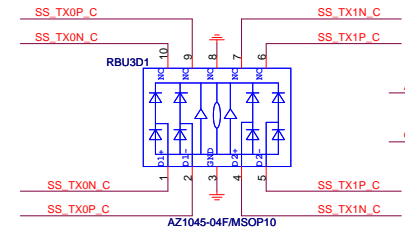
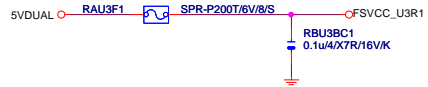
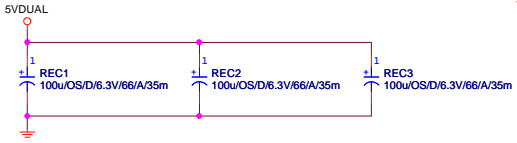
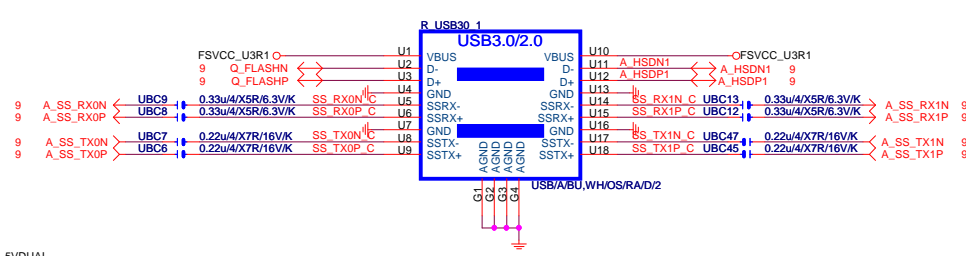
0.22u/4/X5R/6.3V/K, Footprint: C0402-2

EXP A TXP0	PAC4	0.22u/4/X5R/6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4/X5R/6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4/X5R/6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4/X5R/6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4/X5R/6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4/X5R/6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4/X5R/6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4/X5R/6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4/X5R/6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4/X5R/6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4/X5R/6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4/X5R/6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4/X5R/6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4/X5R/6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4/X5R/6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4/X5R/6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4/X5R/6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4/X5R/6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4/X5R/6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4/X5R/6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4/X5R/6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4/X5R/6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4/X5R/6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4/X5R/6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4/X5R/6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4/X5R/6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4/X5R/6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4/X5R/6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4/X5R/6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4/X5R/6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4/X5R/6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4/X5R/6.3V/K	EXP A TXN15C

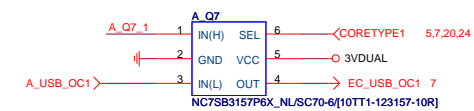
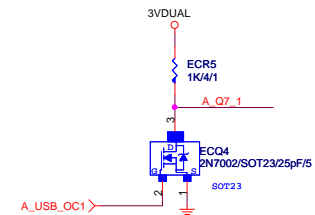
EXP A RXP[0..15] >> EXP\_A\_RXP[0..15] 6  
EXP A RXN[0..15] >> EXP\_A\_RXN[0..15] 6  
EXP A TXP[0..15] >> EXP\_A\_TXP[0..15] 6  
EXP A TXN[0..15] >> EXP\_A\_TXN[0..15] 6



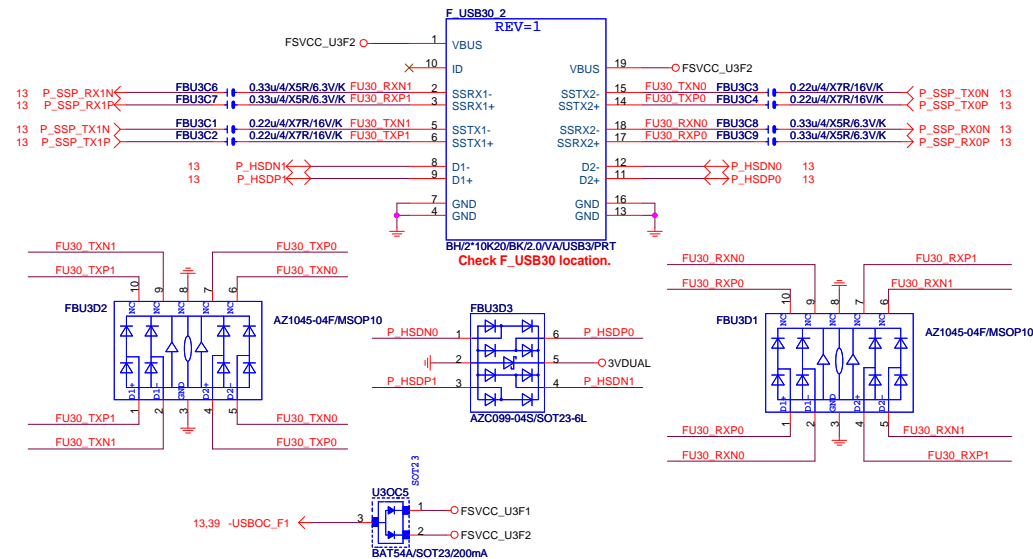
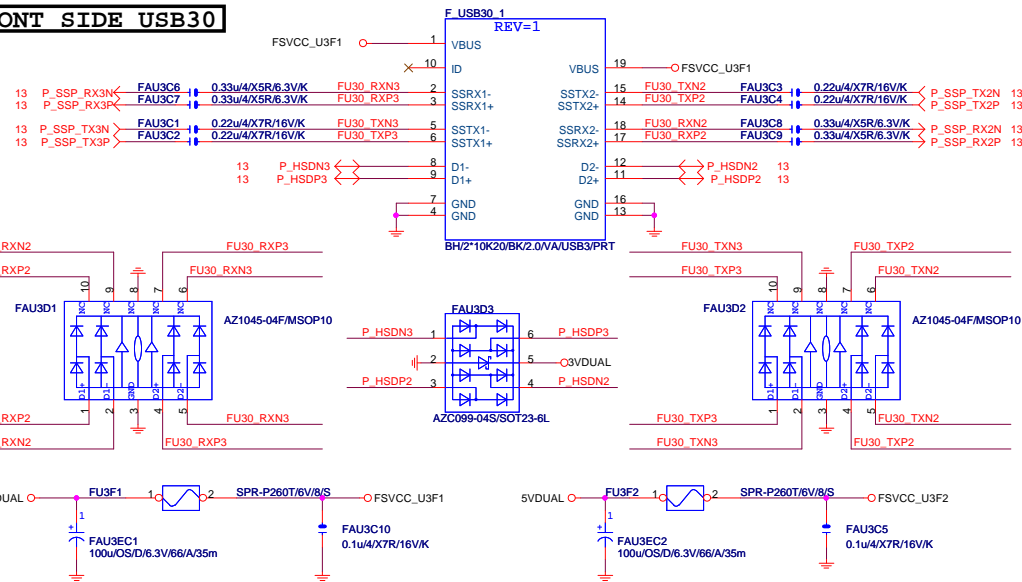


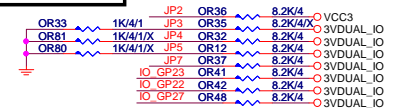


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**FRONT SIDE USB30**





JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

FAN TABLE		
	CPU_FAN	FAN_CTL1 FAN_TAC1
	SYS_FAN1	FAN_CTL2 FAN_TAC2
	SYS_FAN2	FAN_CTL3 FAN_TAC3
	SYS_FAN3	FAN_CTL4 FAN_TAC4
	OPT_FAN OR SYS_FAN4	FAN_CTL5 FAN_TAC5
	THRMTRIP	PIN56
	PROCHOT	PIN89

**DUAL BIOS OPT STRAP**

CN\_N1 OR58 1K/4/1  
OR56 8.2K/4/1/X 3VDUAL\_IO

OR58 上件/OR56 不上件 SINGLE BIOS,  
OR58 不上件/OR56 上件 DUAL BIOS

EMI

## Power leakage

STO 18V

internal power pin, max 22nF cap

SIO CAP

PWR	SHT
-----	-----

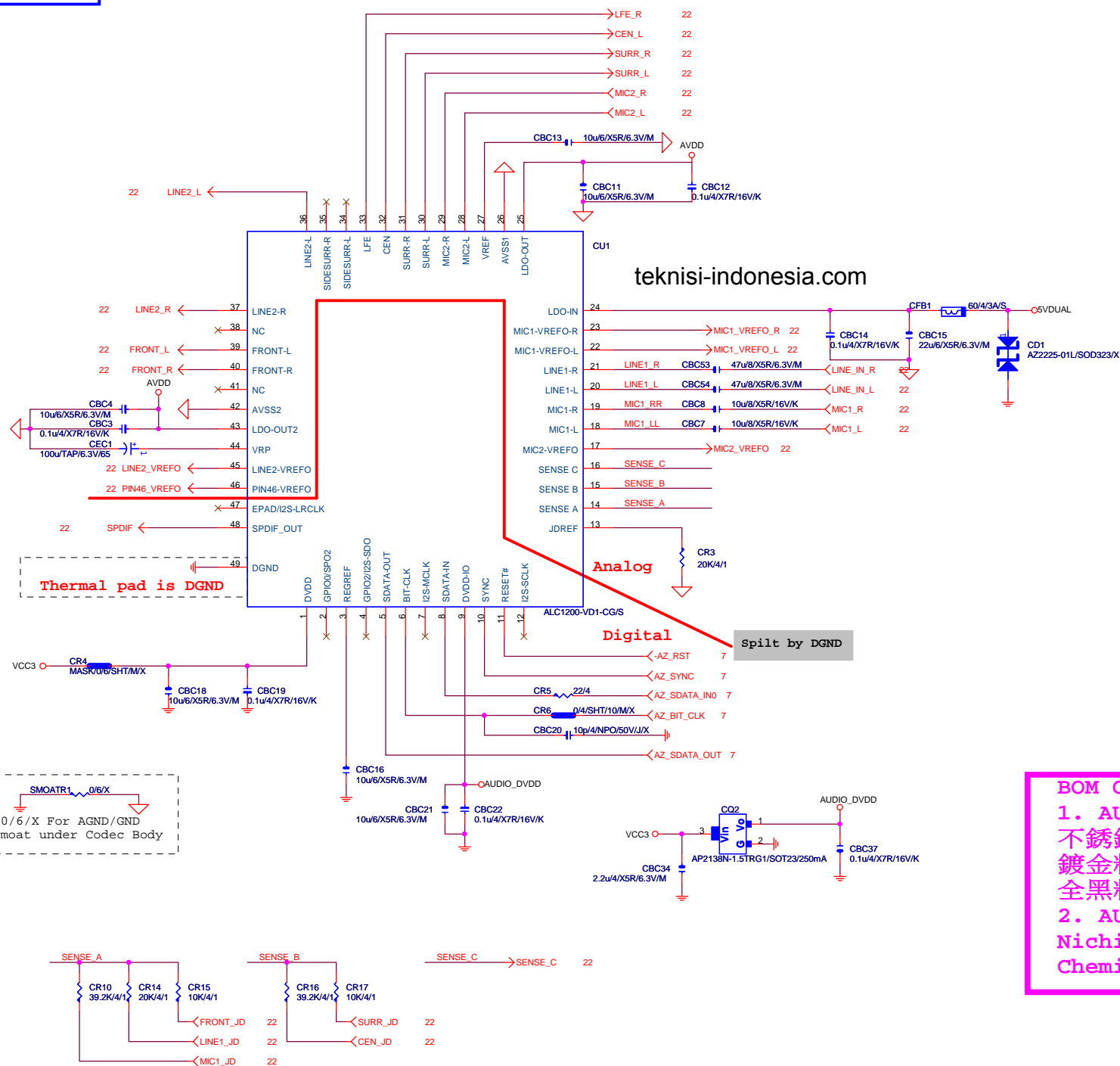
**SIO PU**

**GIGABYTE™**

**ITE 8686 LPC IO, TPM, KB/MS**

Size Custom	Document Number <b>X570 AORUS ELITE</b>	Rev <b>1.0</b>
Date: Thursday, May 30, 2019	Sheet 19 of 55	

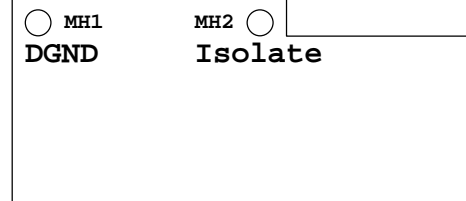
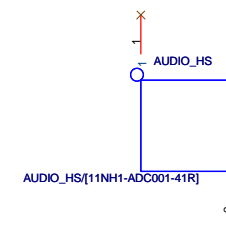
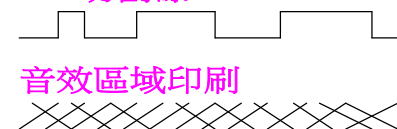




LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND

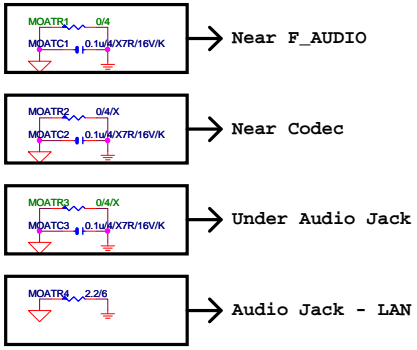
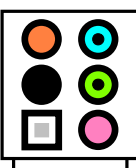
2. MH2一律改為Isolate

LAYOUT注意:是否要加?  
AGND切割線

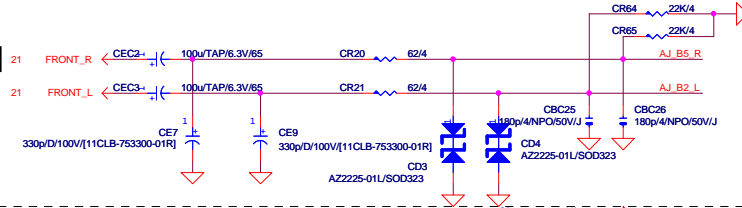
Gigabyte Technology

Title	ALC1220		
Size	Document Number	X570 AORUS ELITE	
Custom		Rev	1.0
Date:	Thursday, May 30, 2019	Sheet	21 of 55

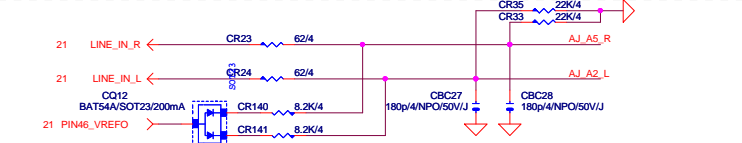
AZALIA JACK



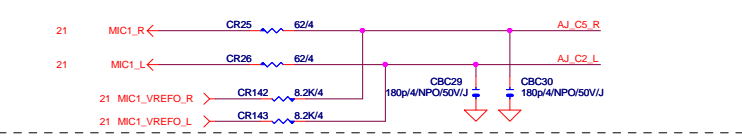
LINE-OUT



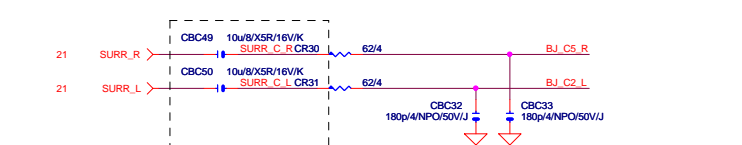
LINE-IN



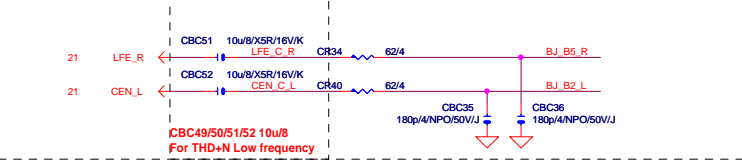
MIC-IN



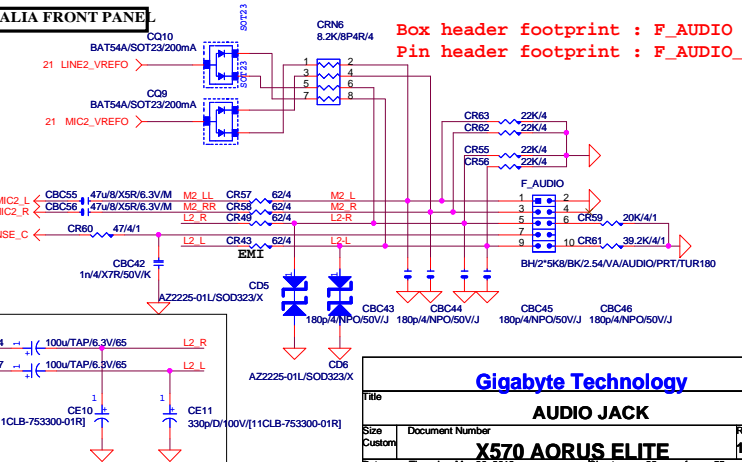
SURROUND



CEN/LFE

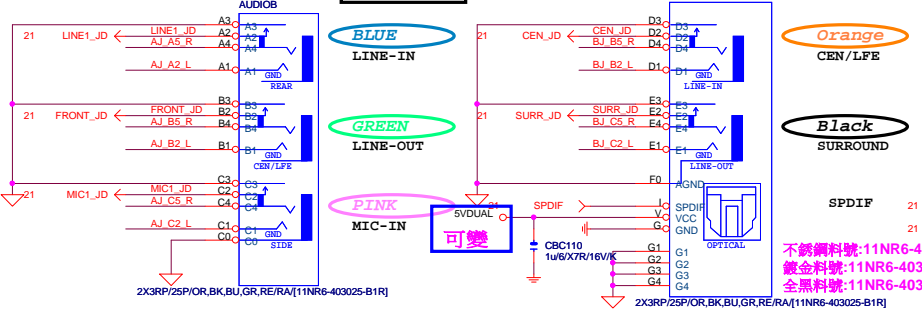


AZALIA FRONT PANE



Box header footprint : F\_AUDIO  
Pin header footprint : F\_AUDIO\_S

AZALIA JACK



Orange  
CEN/LFE

Black  
SURROUND

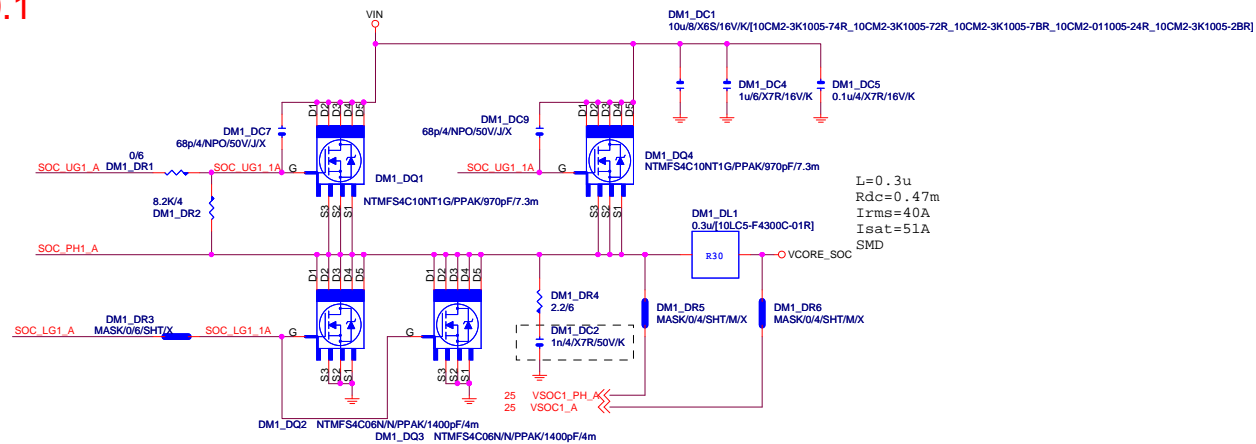
SPDIF

不銹鋼料號:11NR6-403025-A3R  
鍍金料號:11NR6-403025-92R  
全黑料號:11NR6-403025-B1R

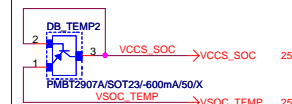
Gigabyte Technology

File		
AUDIO JACK		
Size	Document Number	Rev
Custom	X570 AORUS ELITE	1.0
Date:	Thursday, May 30, 2019	Sheet 22 of 55

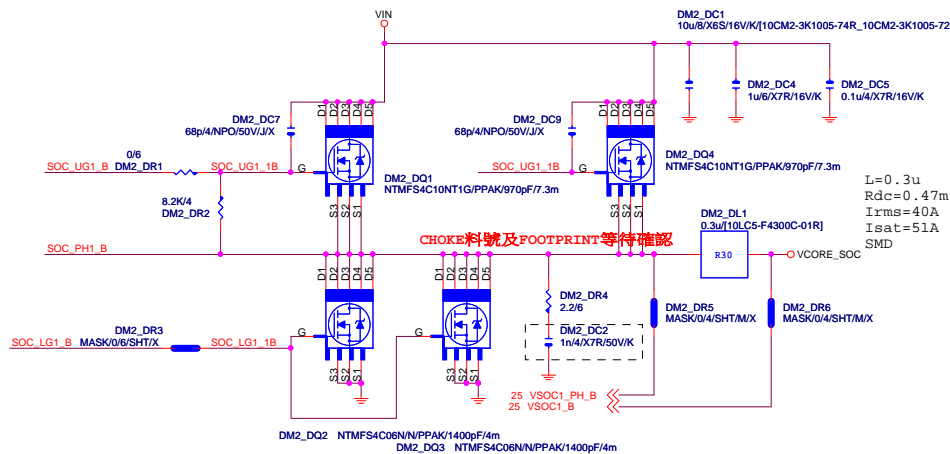
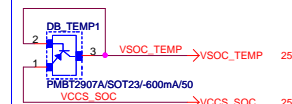
REV:0.1



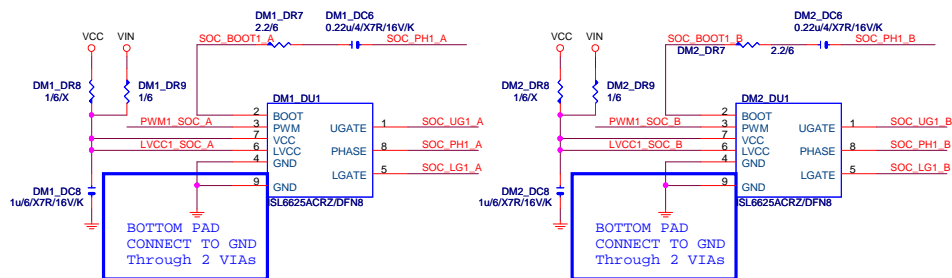
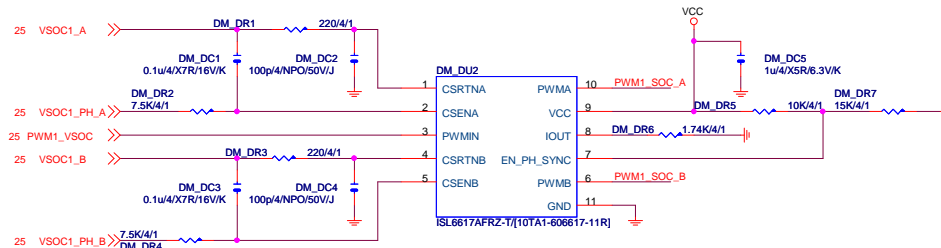
Place near hot area



Place near to DGL1



CHOKES料號及FOOTPRINT等待確認



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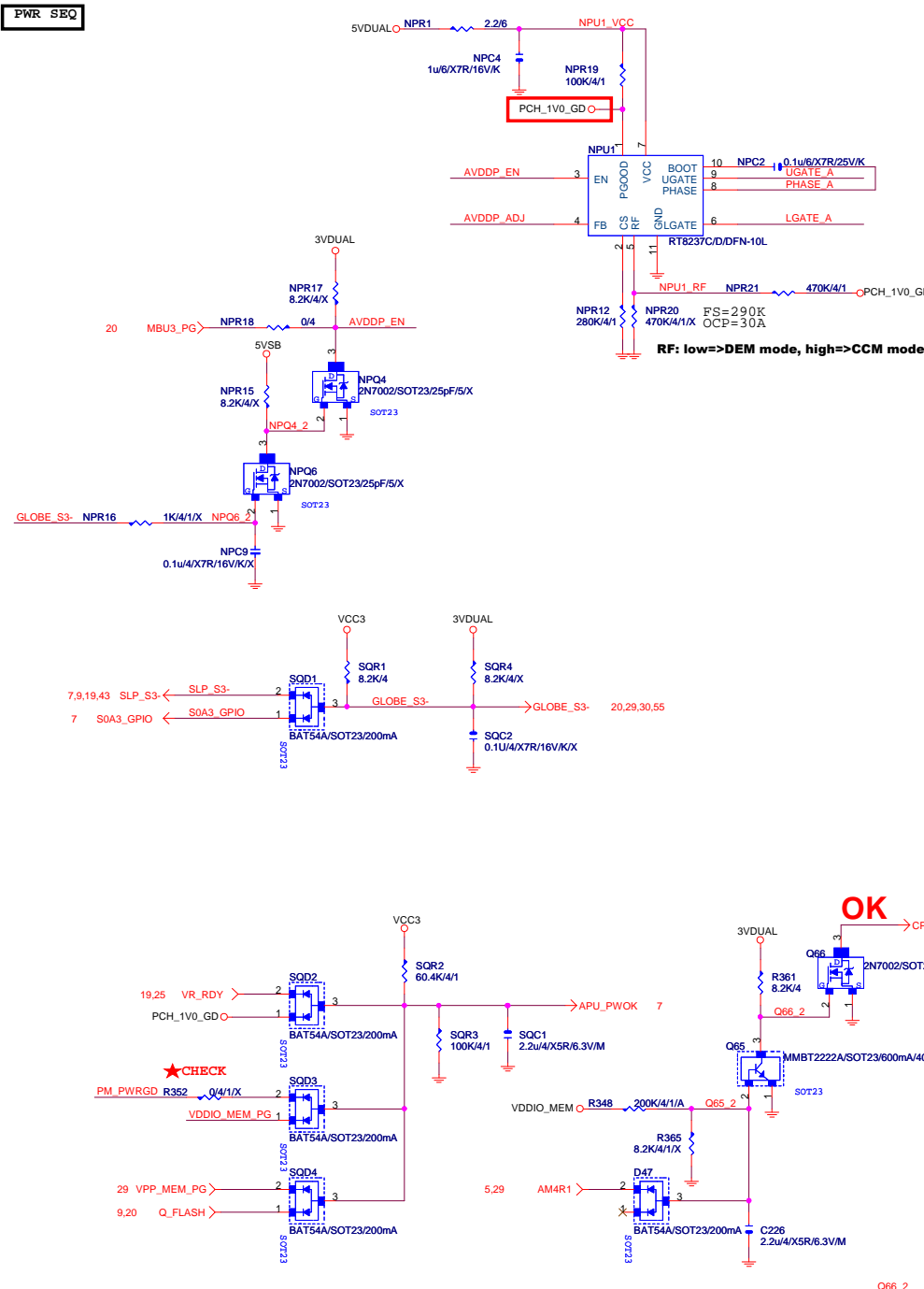
VCORE MOS

Document Number X570 AORUS ELITE

Date: Thursday, May 30, 2019

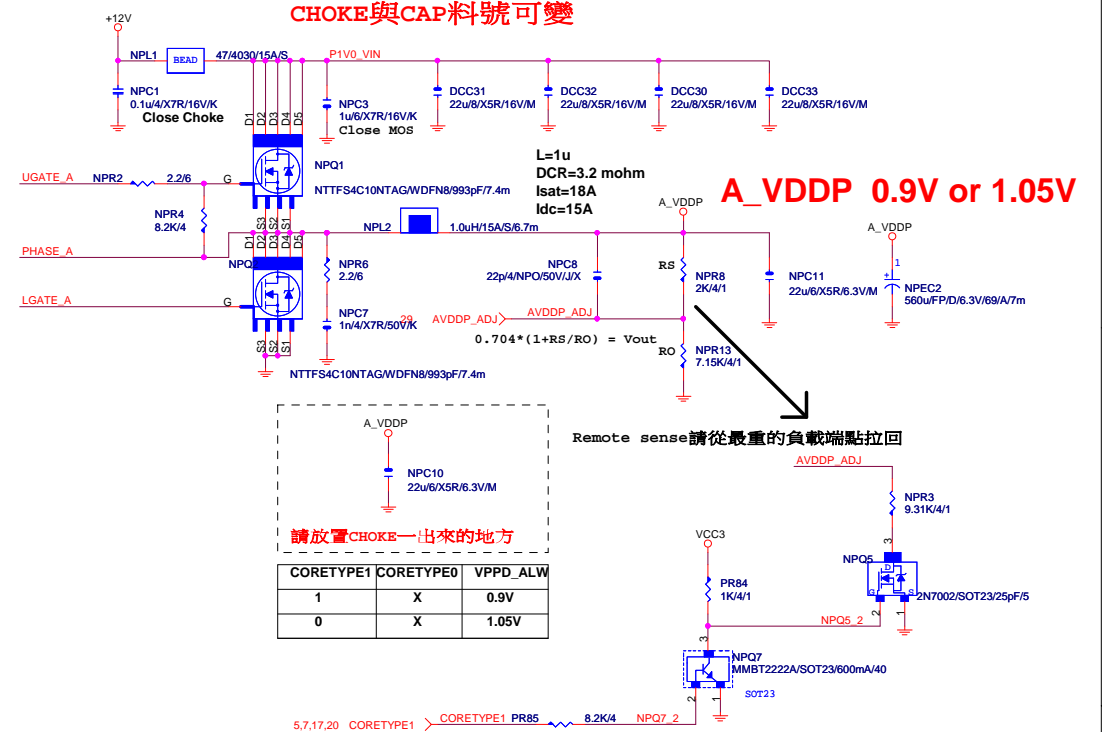
Sheet 23 of 55

Rev 1.0



RF: low=>DEM mode, high=>CCM mode.

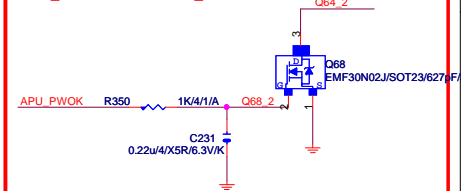
# CHOKE與CAP料號可變



請放置CHOKE一出來的地方

## ★Sequence

APU\_PWOK control PM\_PWGRD

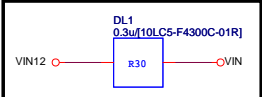
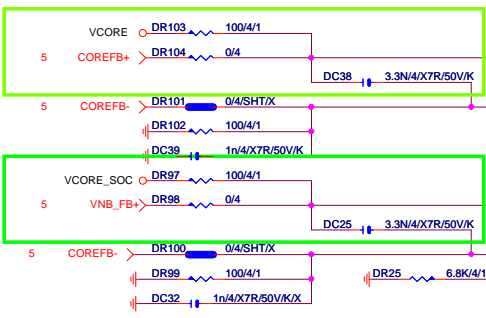
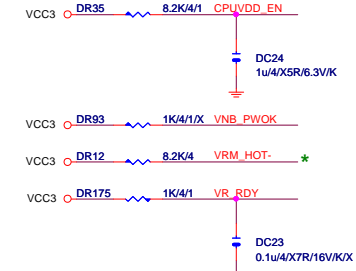
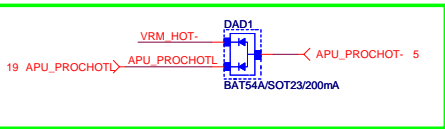


GIGABYTE™

POWER SEQUENCE		
Title	Document Number	Rev
Size	Custom	1.0
Date: Thursday, May 30, 2019	Sheet 24	of 55

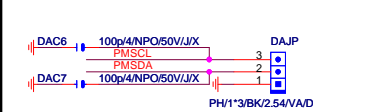
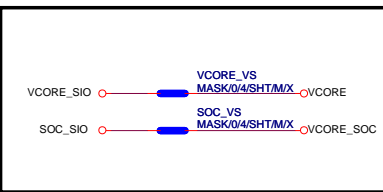
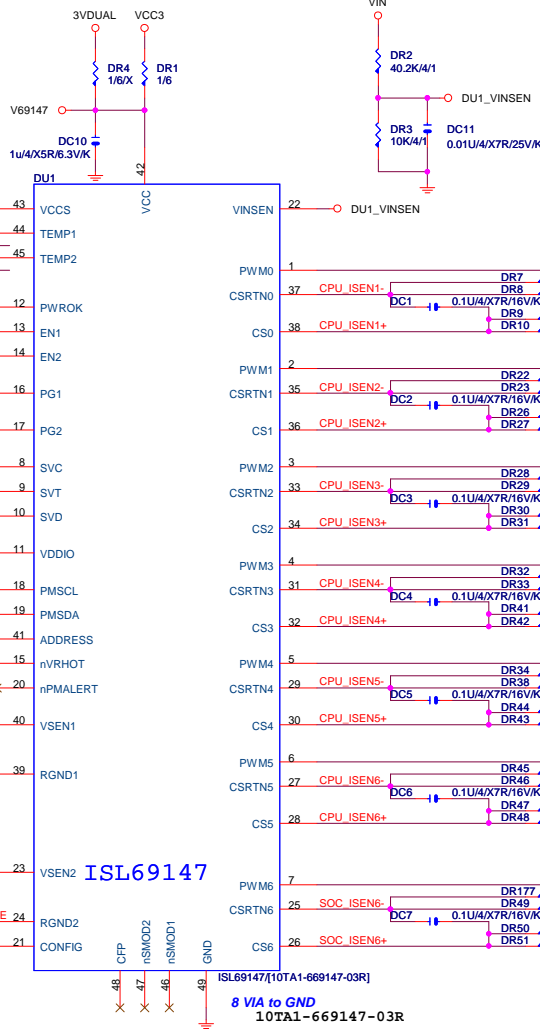
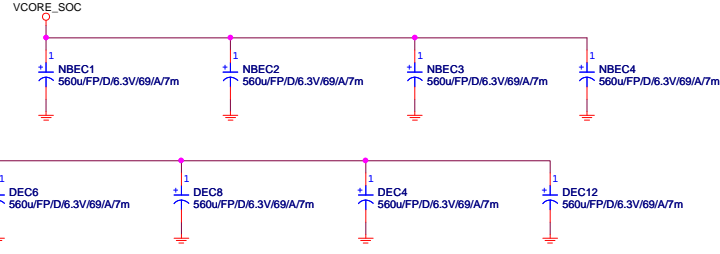
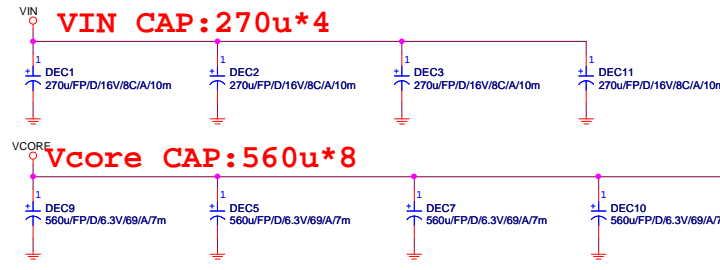


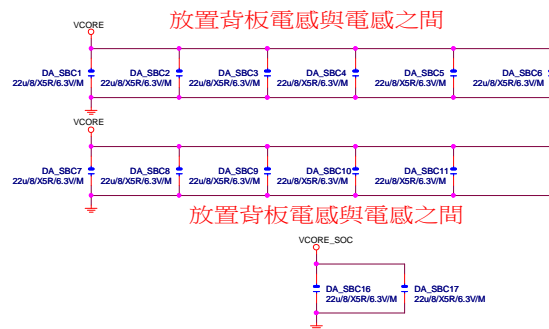
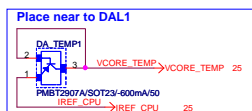
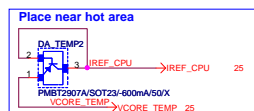
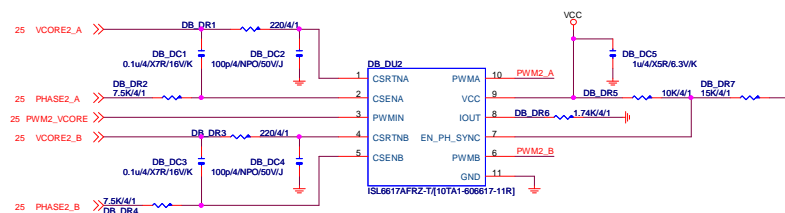
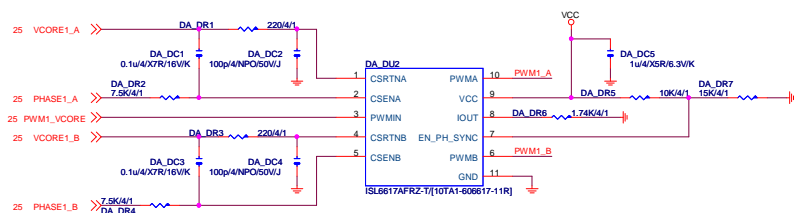
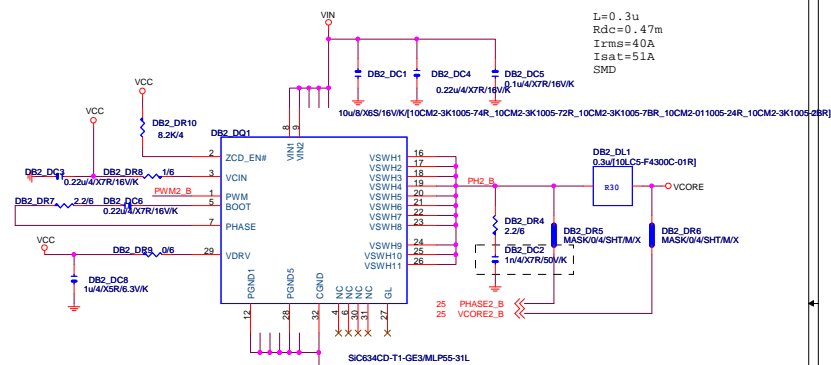
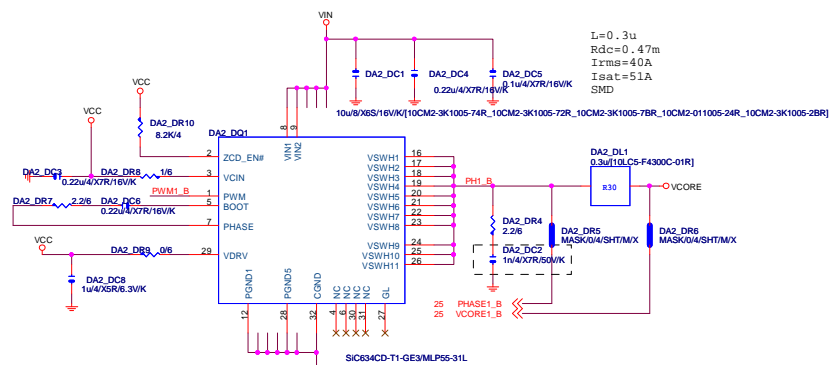
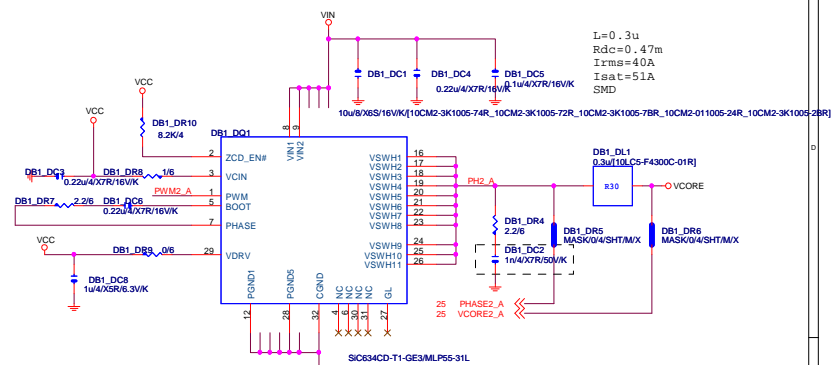
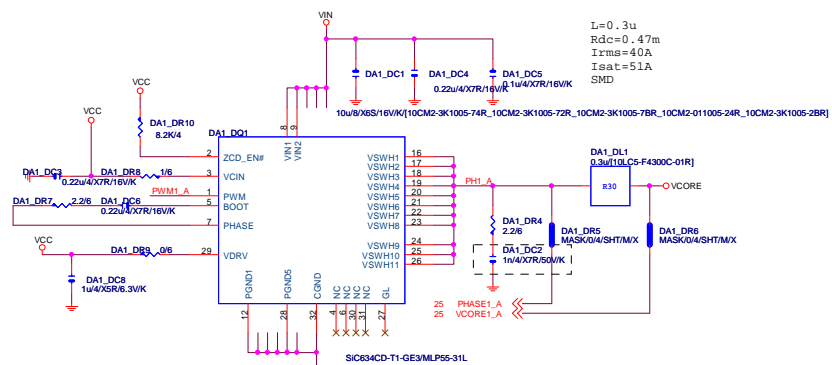
REV:0.1

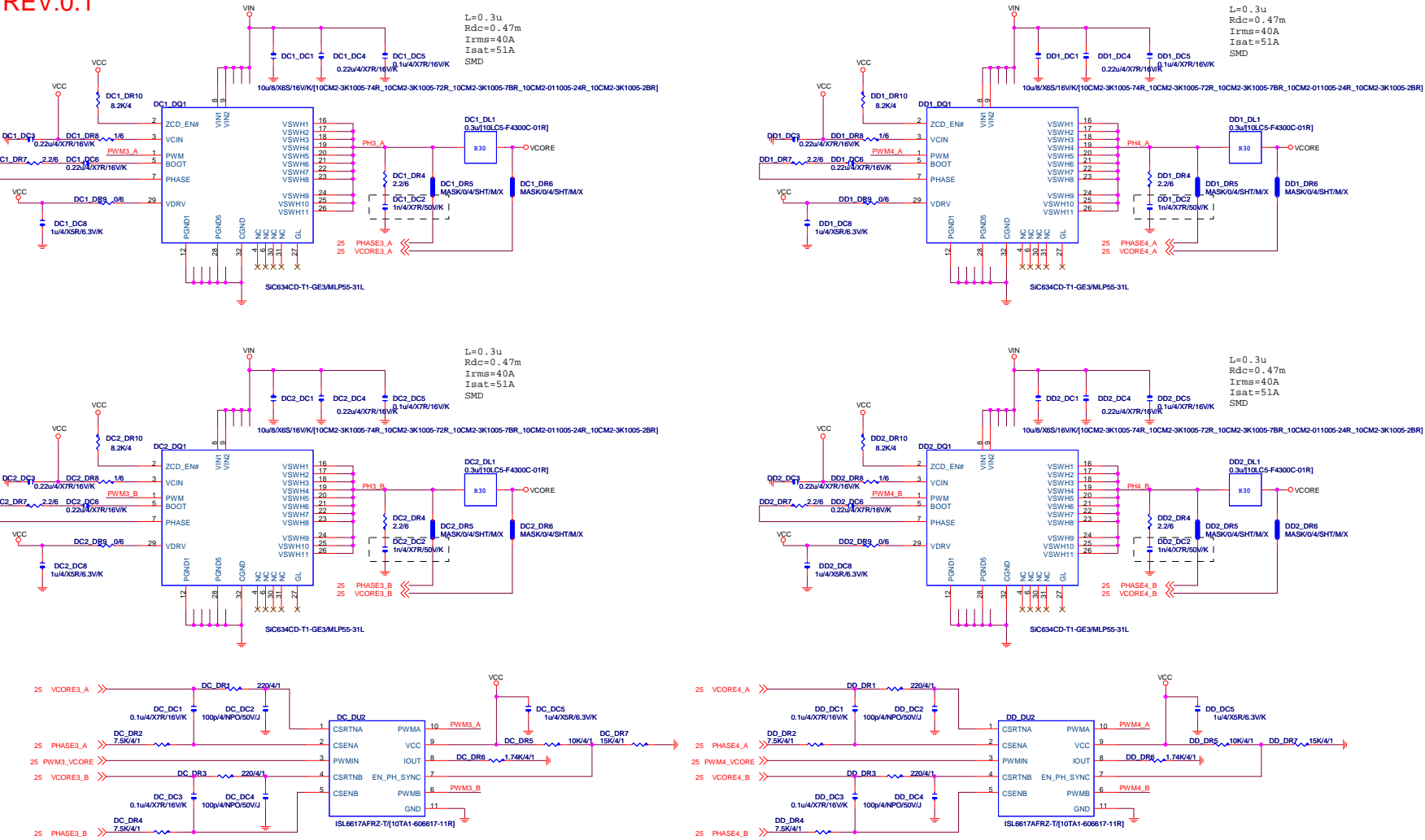


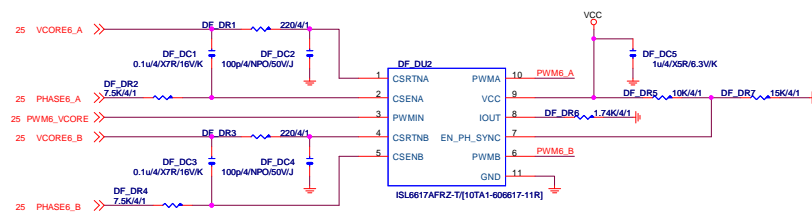
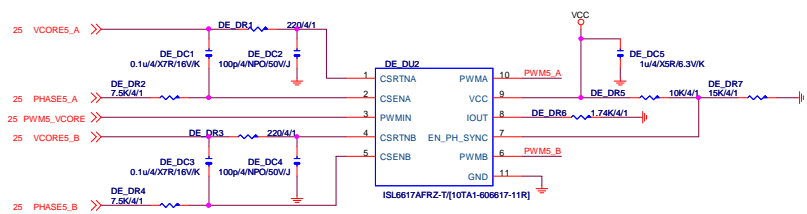
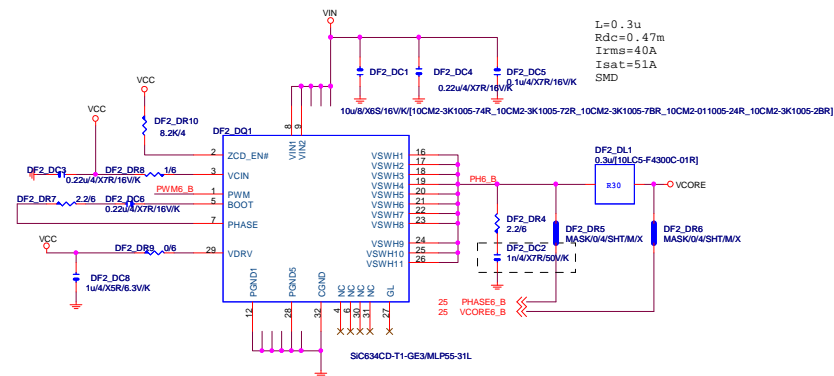
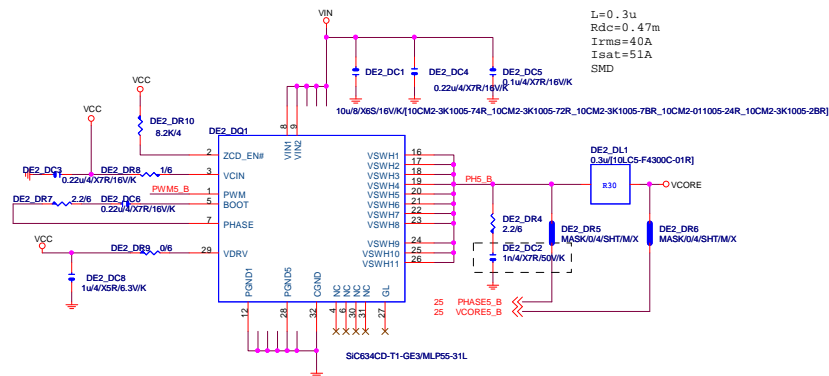
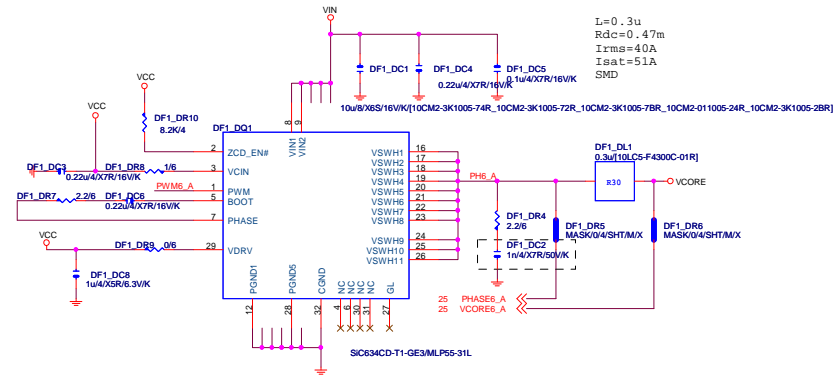
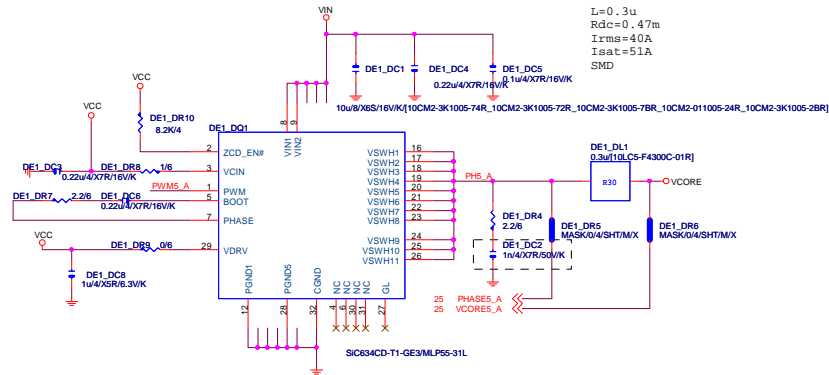
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Vcore\_SOC CAP:560u\*4

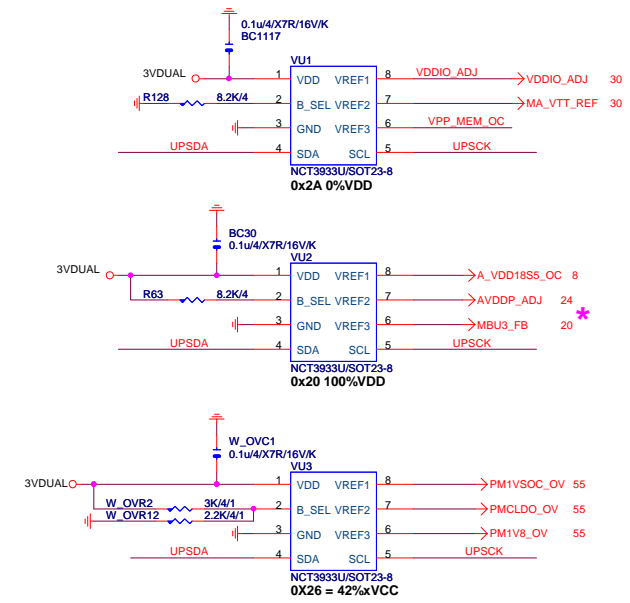
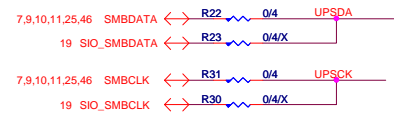
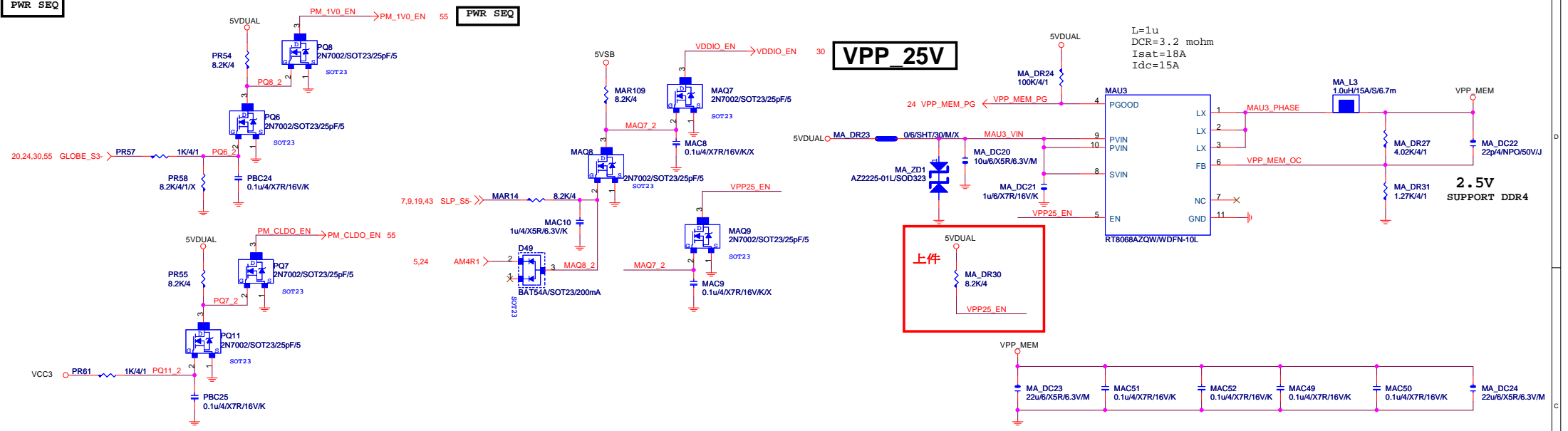








VPP\_25V



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

**GIGABYTE™**

Title

PM POWER

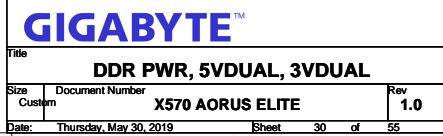
Size Custom

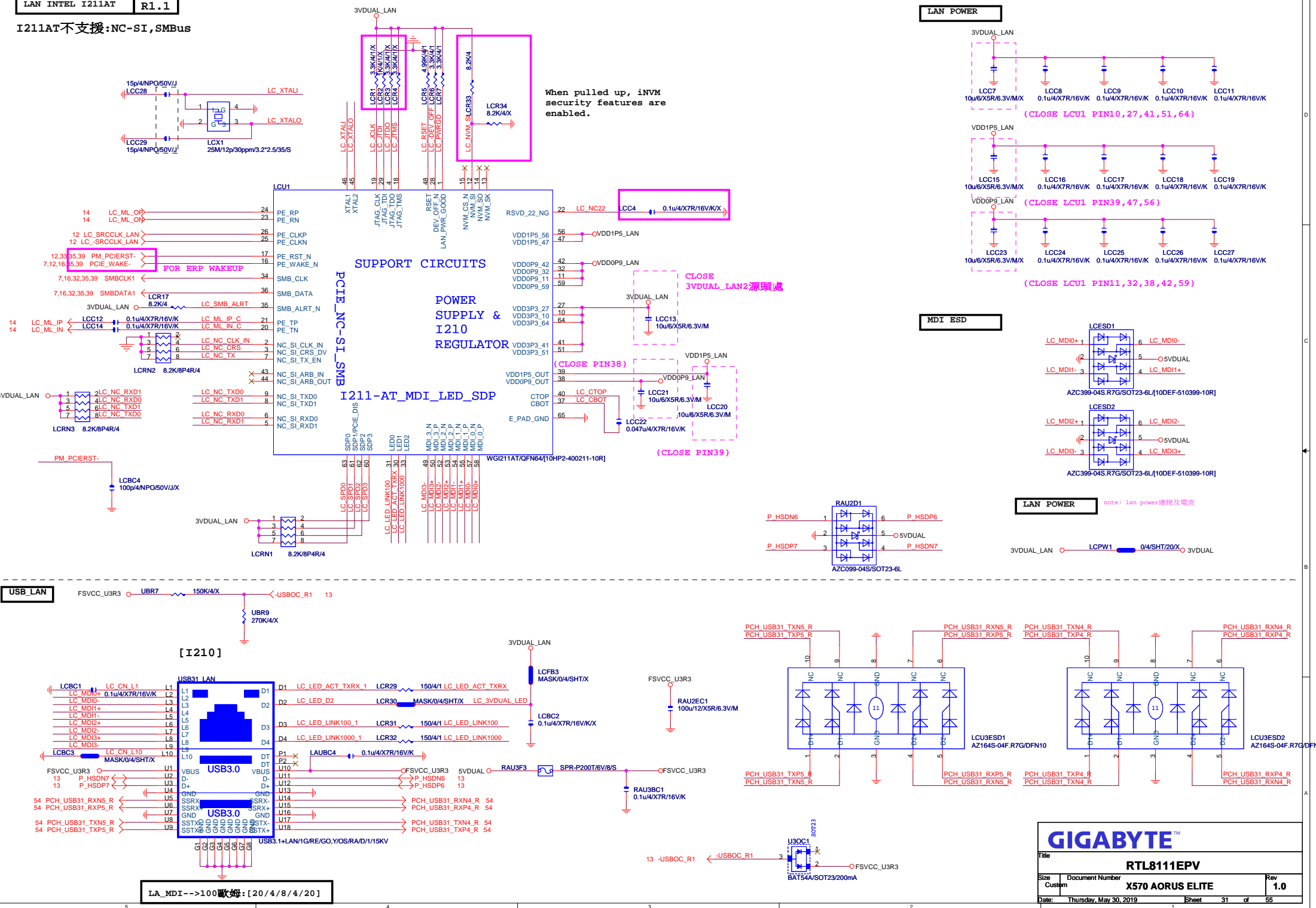
Document Number X570 AORUS ELITE

Date: Thursday, May 30, 2019

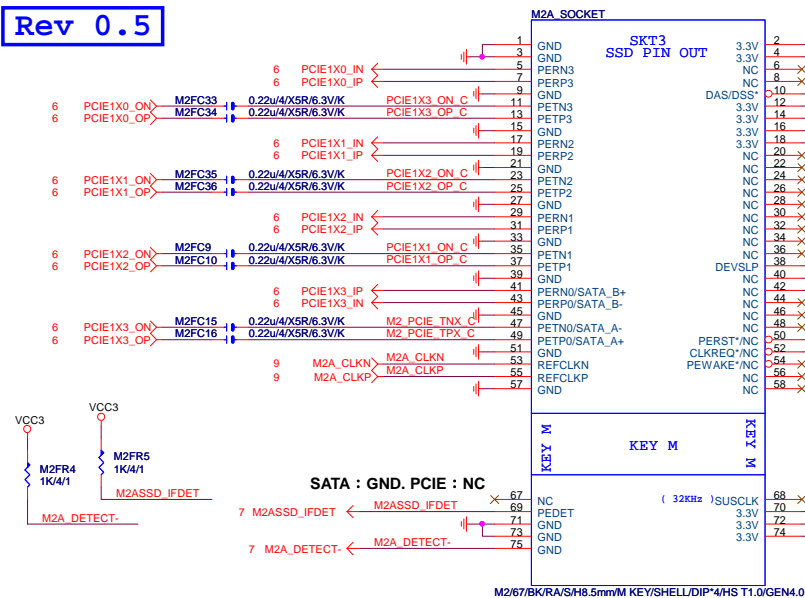
Sheet 29 of 55

Rev 1.0



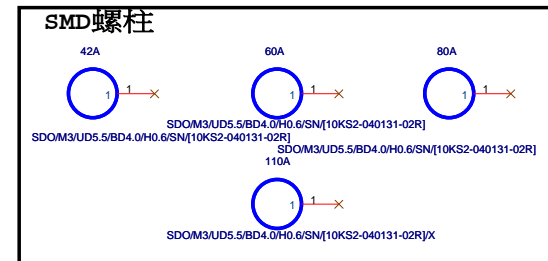
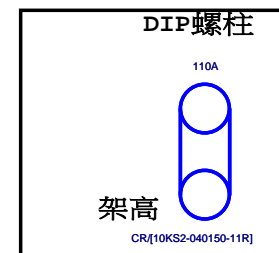
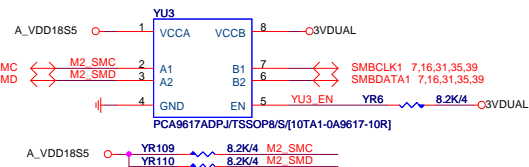
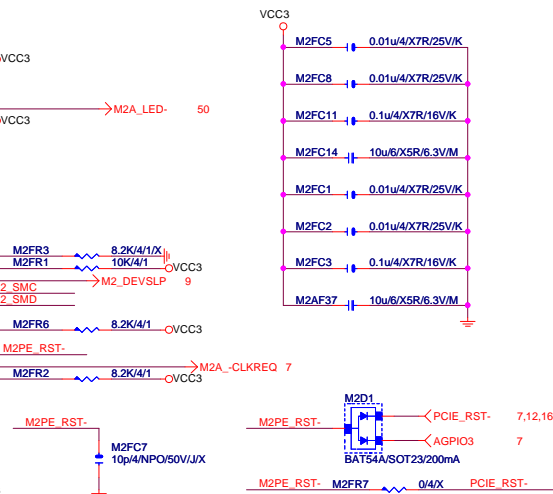


Rev 0.5

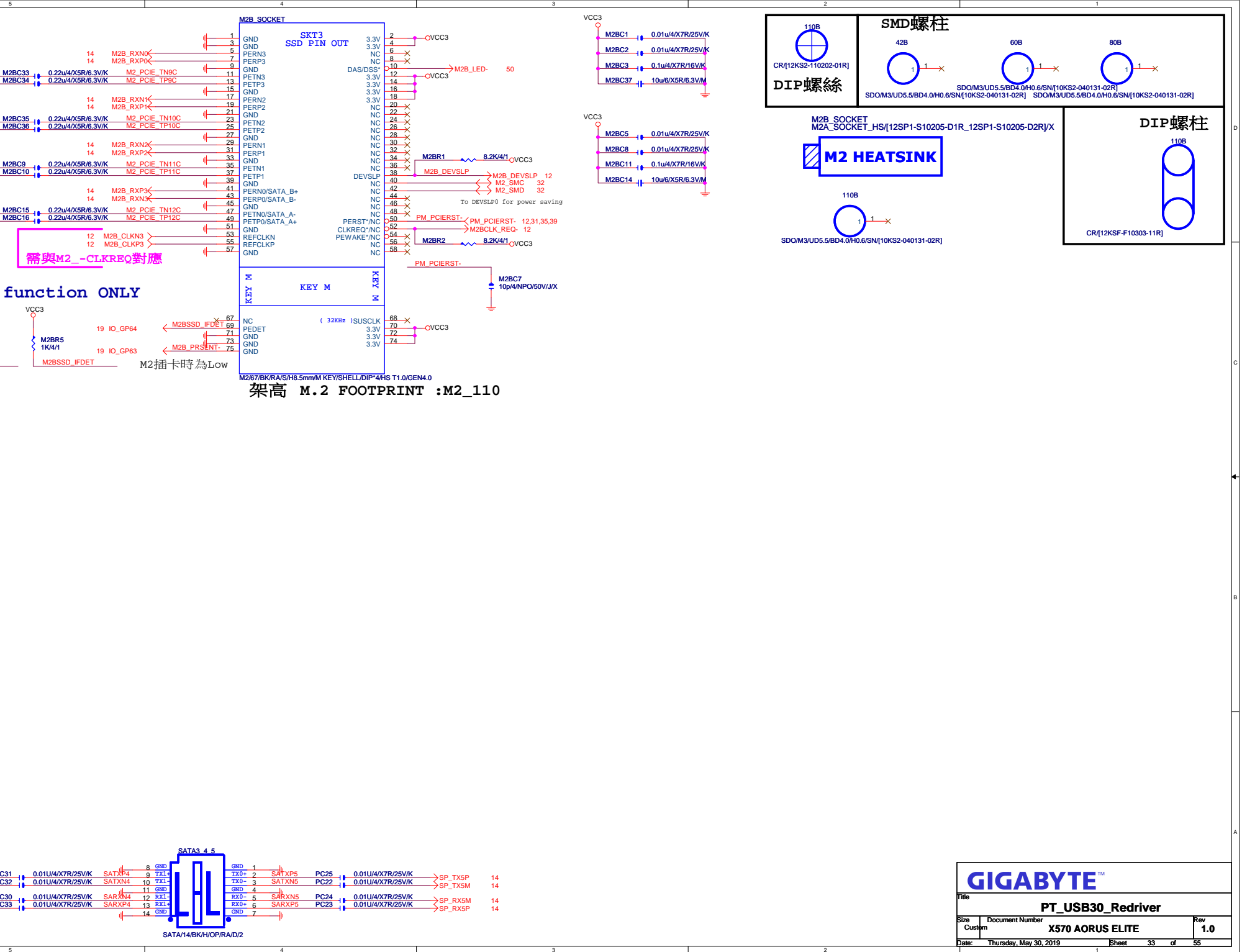
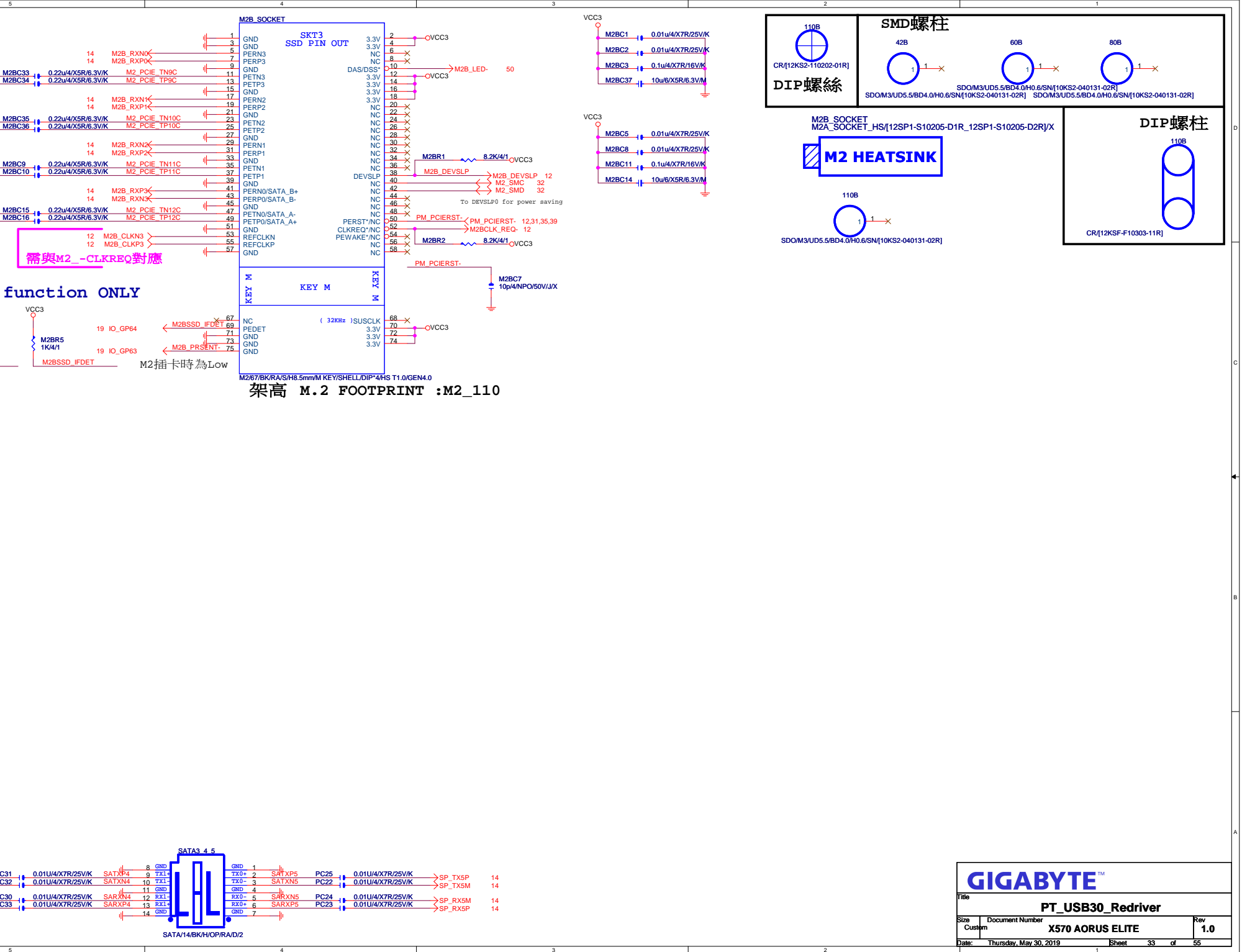


M2/67/BK/RA/S/H8.5mm/M KEY/SHELL/DIP\*4/HS T1.0/GEN4.0

8.5H鐵殼  
Footprint :M2\_110(DIP)

M2A\_SOCKET  
M2A\_SOCKET\_HS/[12SP1-S10205-D1R\_12SP1-S10205-D2R] **M2 HEATSINK**



[illegible]

**M2 SOCKET**

**SKT3 SSD PIN OUT**

**需與M2-CLKREQ對應**

**function ONLY**

**需與M2-CLKREQ對應**

**M2插卡時為Low**

**M2\_110**

**SATA3 4 5**

**SATA14/BK/HOP/RA/D/2**

**M2B\_SOCKET**

**M2A\_SOCKET\_HS[12SP1-S10205-D1R\_12SP1-S10205-D2R]/X**

**M2 HEATSINK**

**DIP螺絲**

**DIP螺柱**

**DIP螺柱**

**GIGABYTE™**

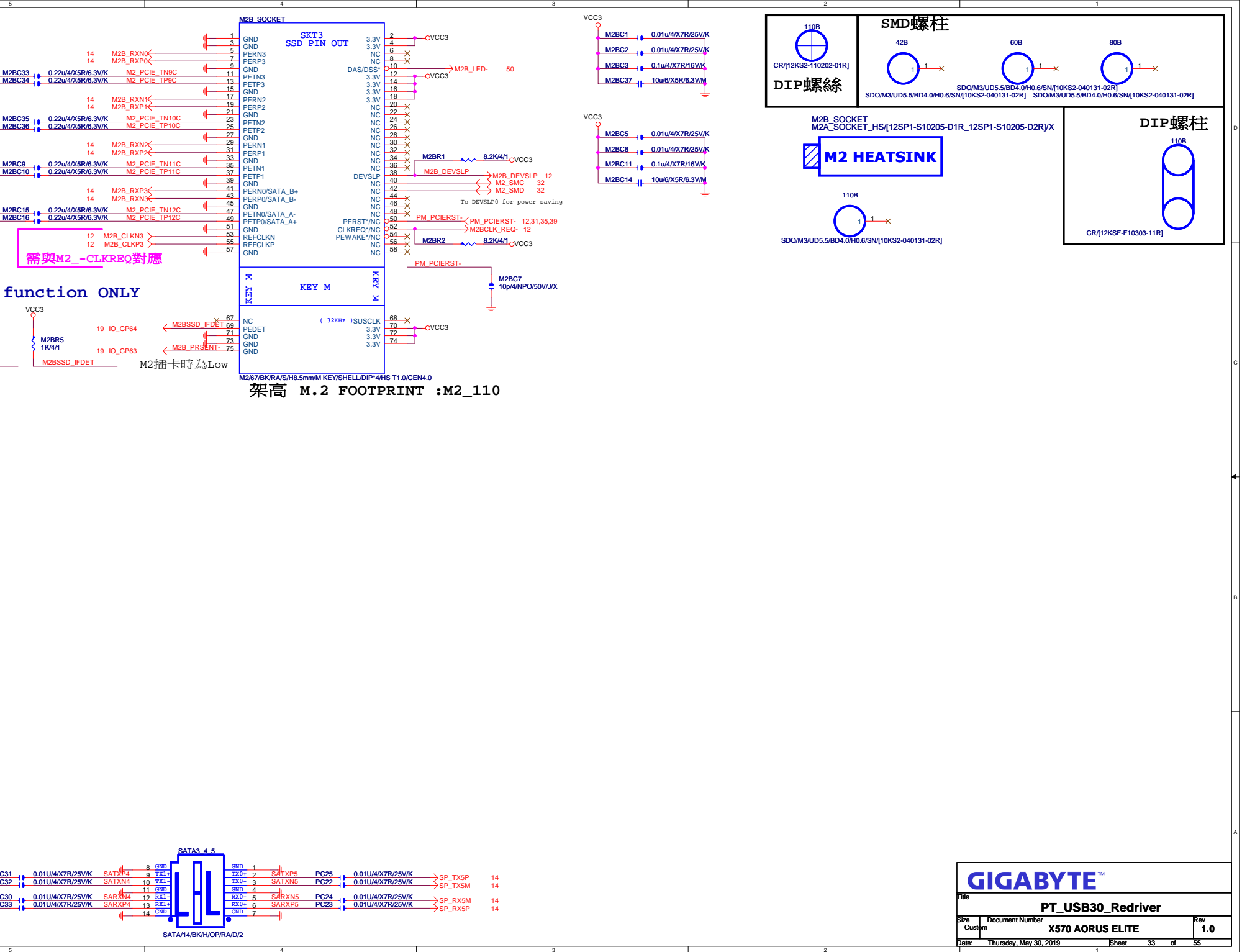
**PT\_USB30\_Redriver**

**X570 AORUS ELITE**

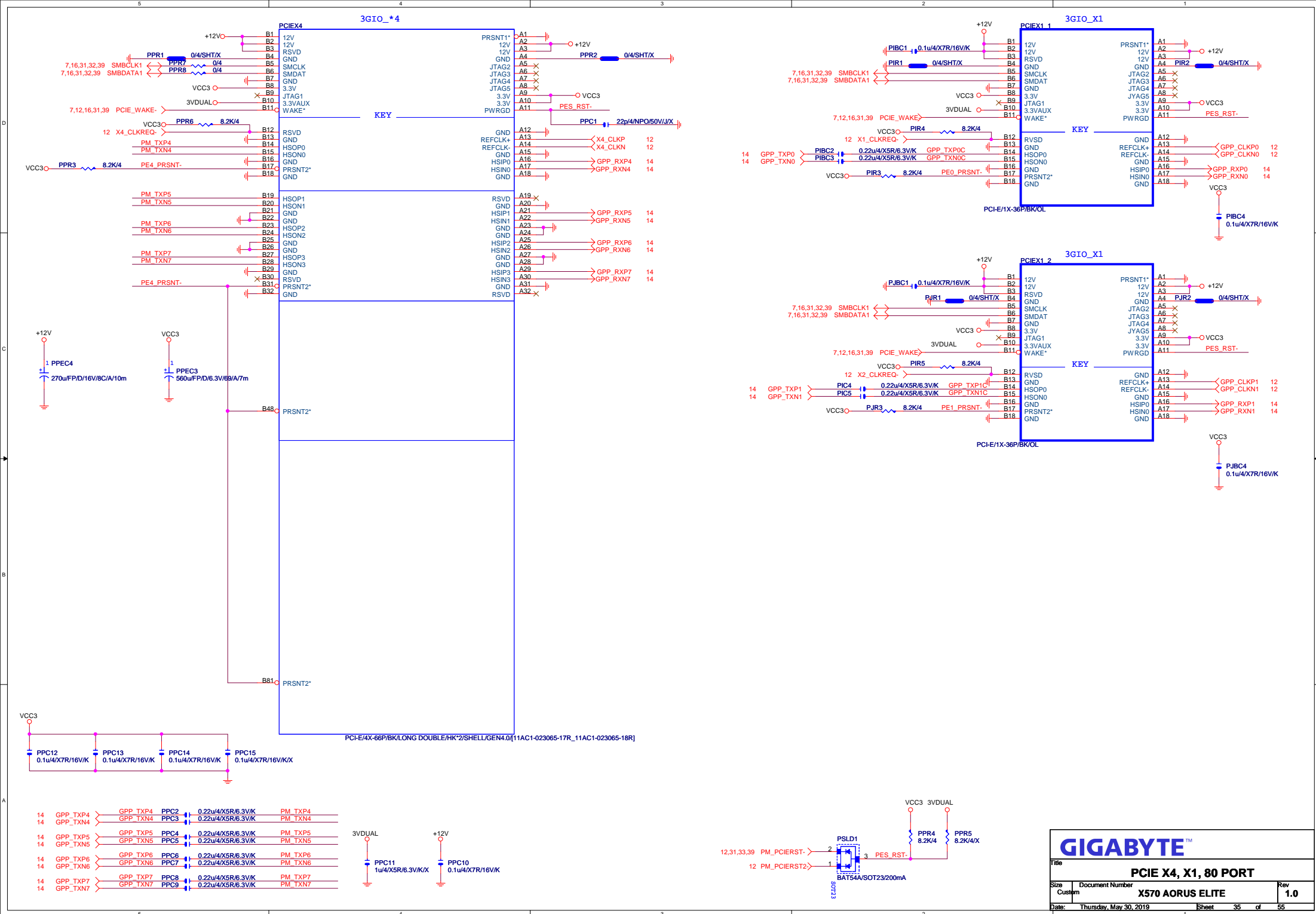
**Rev 1.0**

**Date: Thursday, May 30, 2019**

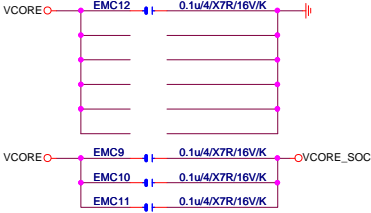
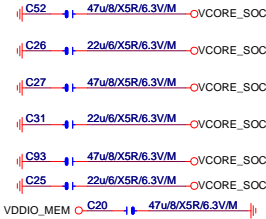
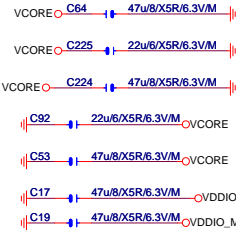
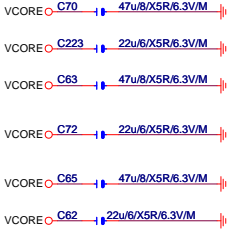
**Sheet 33 of 55**



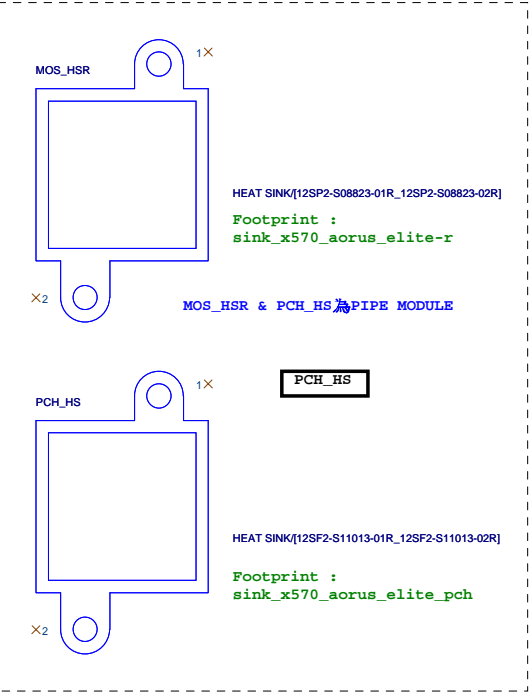
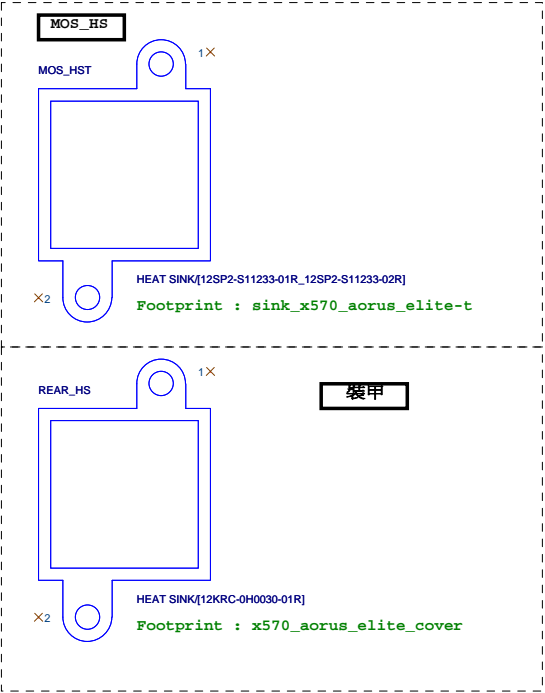
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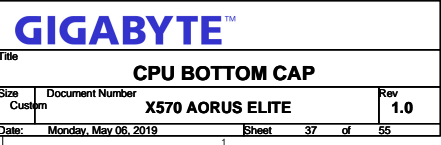


CPU TOP CAVITY



Cross Plane CAP





D

C

B

A

**GIGABYTE™**

[illegible]

## M.2 SOCKET

Size	
Cu	

Custom

Document Number
-----------------

**X570 AORUS ELITE**

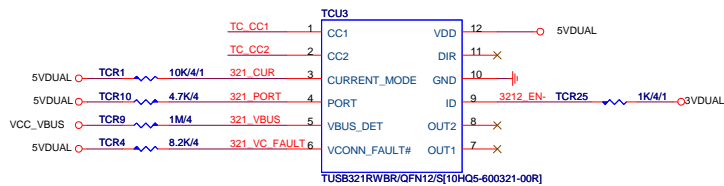
Rev	1.0
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1.0

Date: Monday, May 06, 2019

Sheet 38 of 55

## Front U31 w/ TI HD3SS3220



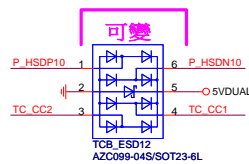
### CURRENT MODE

L - Default current / Pull down to GND or NC  
M - Medium (1.5A) current / Pull up to VDD 500K  
H - High (3.0A) current / Pull up to VDD 10K

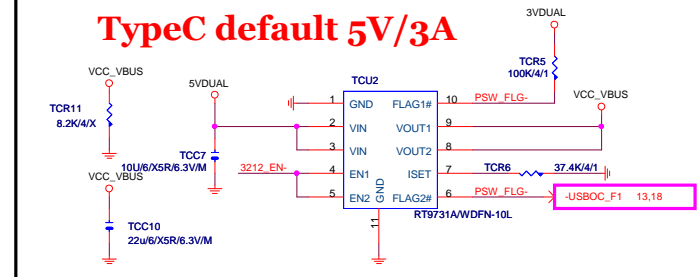
### PORT

H - HOST  
L - Device  
NC - Dual Role

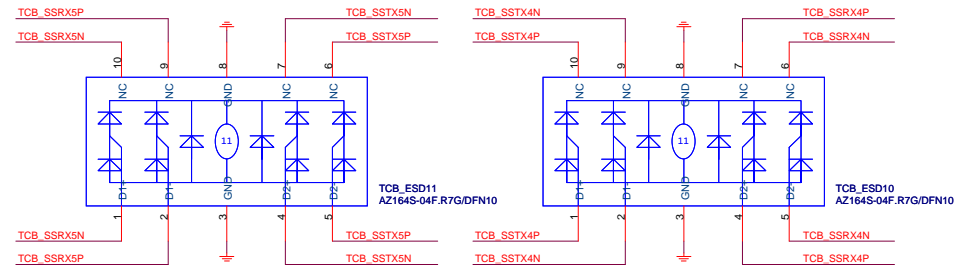
note:可變更USB NAME



## TypeC default 5V/3A



## Color markers can be changed by model



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Rev: 0.2

請選擇適用的USBPort :  
SOC/UD7/UD5/G1/G7 : USB4  
UD3/G5:USB6

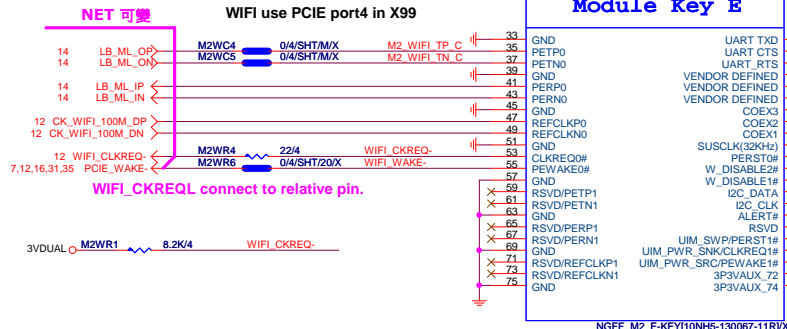
NET 可變

PCIE:15/4/4/15(breakout min 8/4/4/8)  
外層Impedance=85 + 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)  
內層Impedance=85 + 12%

WIFI use PCIE port4 in X99

Module Key E



### Footprint Notice.

★Update 2015-07-22

★Footprint for  
直立式 SMD:  
WIFI-EKEY

### Footprint Notice.

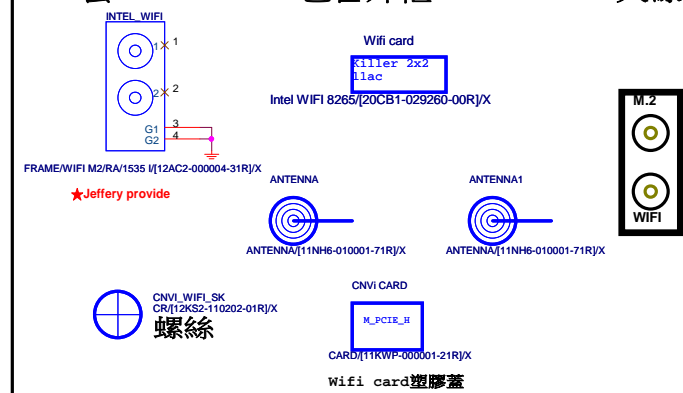
★Update 2015-07-22

★Footprint for 橫躺式 SMD:  
NGFF-E-75P-2

FOR M.2 WIFI MODULE @ REAR PANEL

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



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M.2, F_TYPE C		
Size	Document Number	Rev
Custom	X570 AORUS ELITE	1.0
Date:	Thursday, May 30, 2019	Sheet 39 of 55

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	

<b>GIGABYTE™</b>		
Title <b>M.2 SOCKET</b>		
Size Custom	Document Number <b>X570 AORUS ELITE</b>	Rev <b>1.0</b>
Date: Monday, May 06, 2019	Sheet 40 of 55	1



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	

<b>GIGABYTE™</b>		
Title <b>M.2 SOCKET</b>		
Size Custom	Document Number <b>X570 AORUS ELITE</b>	Rev <b>1.0</b>
Date: Monday, May 06, 2019	Sheet 41 of 55	1

D

C

B

A



Title	Author	Date	Page No.

### PCIE X8, SWITCH

Size	
Cu	

Custom

Document Number
-----------------

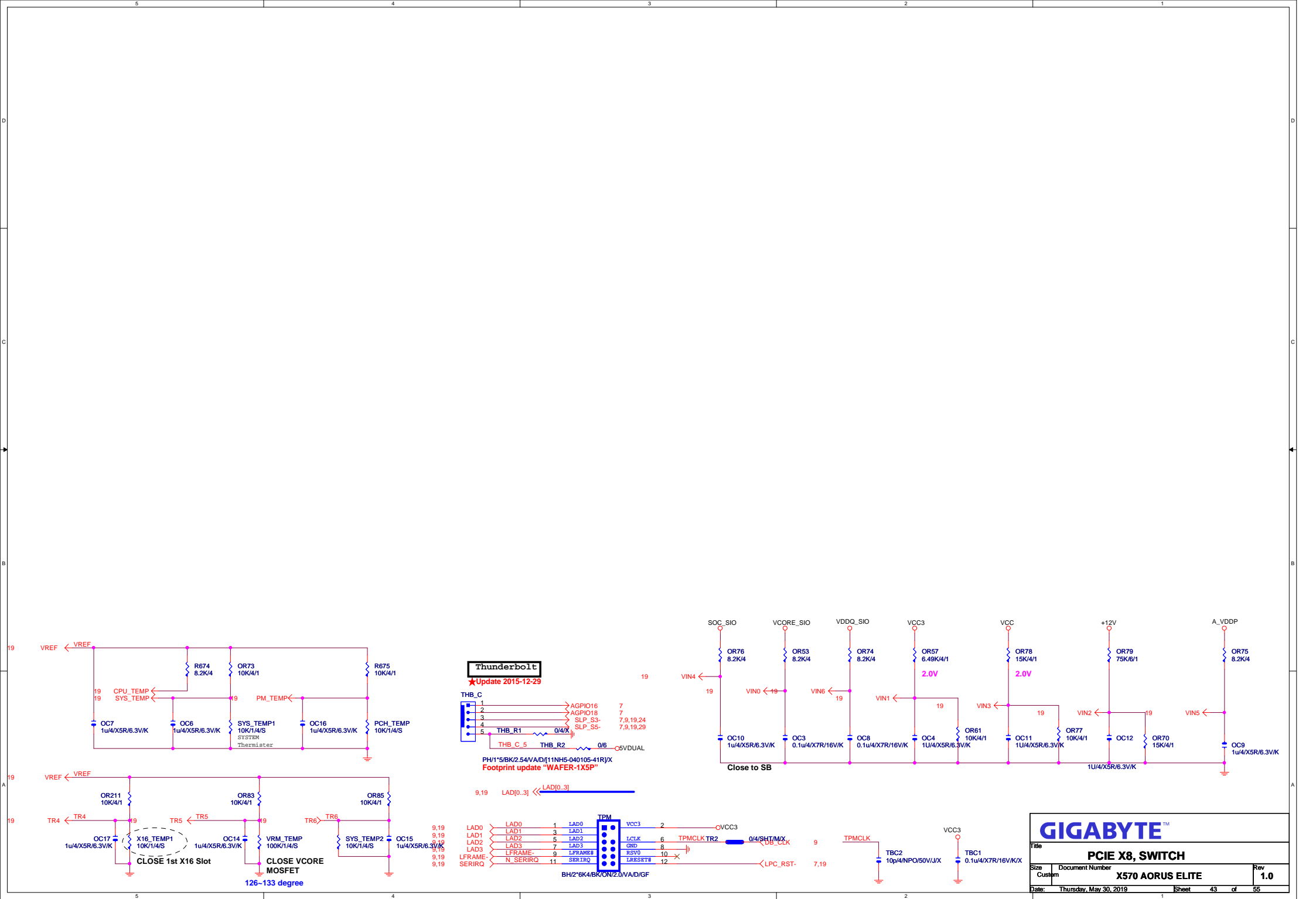
**X570 AORUS ELITE**

Rev	1.0
-----	-----

1.0

Date: Monday, May 06, 2019

Sheet 42 of 55





<b>GIGABYTE™</b>		
Title <b>DIGITAL LED</b>		
Size Custom	Document Number <b>X570 AORUS ELITE</b>	Rev <b>1.0</b>
Date: Monday, May 06, 2019	Sheet 44	of 55

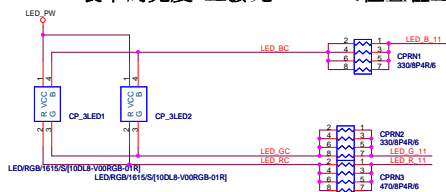


**GIGABYTE™**

Title			ASM 2142 U31		
Size	Document Number				Rev
Custom	X570 AORUS ELITE				1.0
Date:	Monday, May 06, 2019		Sheet	45 of	55

## 第一區 LED

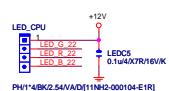
FOR 裝甲高亮度 正發光 LED\*2 (位置在正板,依據裝甲設計擺放)



FOOTPRINT: LED\_4P\_RGB高亮度

## 第二區 LED

燈條 LED (LED\_CPU放在CPU附近位置)

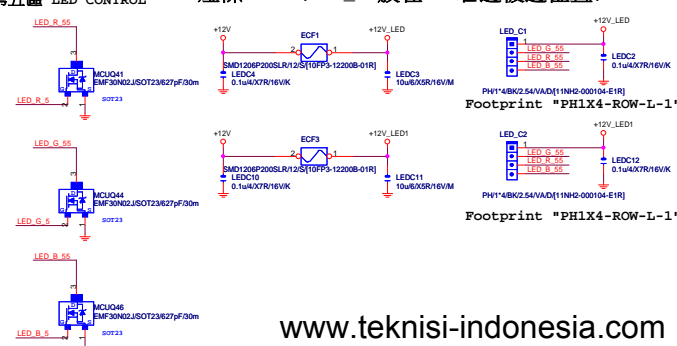


Footprint "PH1X4-FAN-AMD-L"

## 第五區 LED

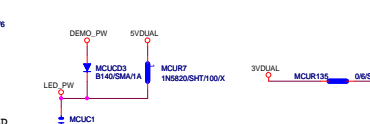
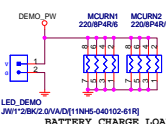
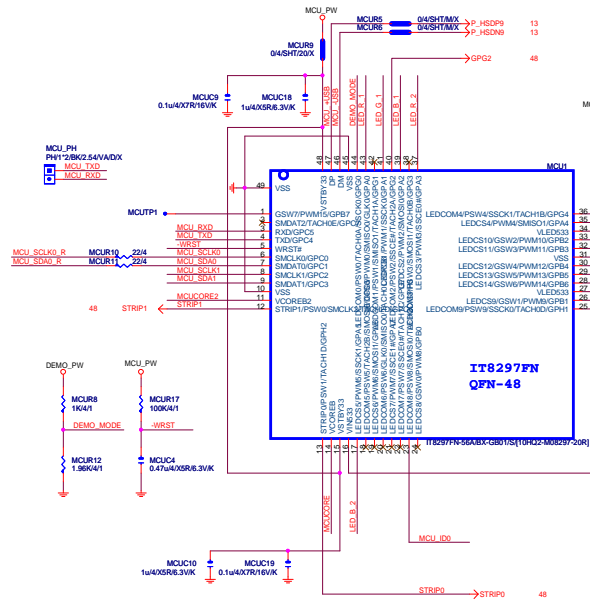
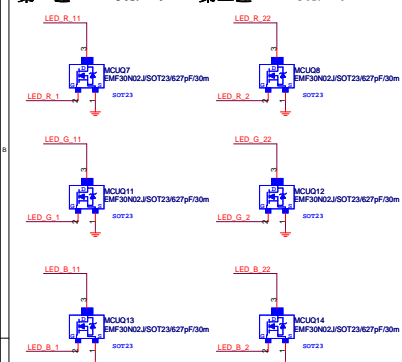
燈條 LED (LED\_C1放在PCB左邊板邊位置)

燈條 LED (LED\_C2放在PCB右邊板邊位置)



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## 第一區 LED CONTROL 第二區 LED CONTROL



For AMD MCU update

SEL	Y+	Y-
L	M+	M-
H	D+	D-

Default SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

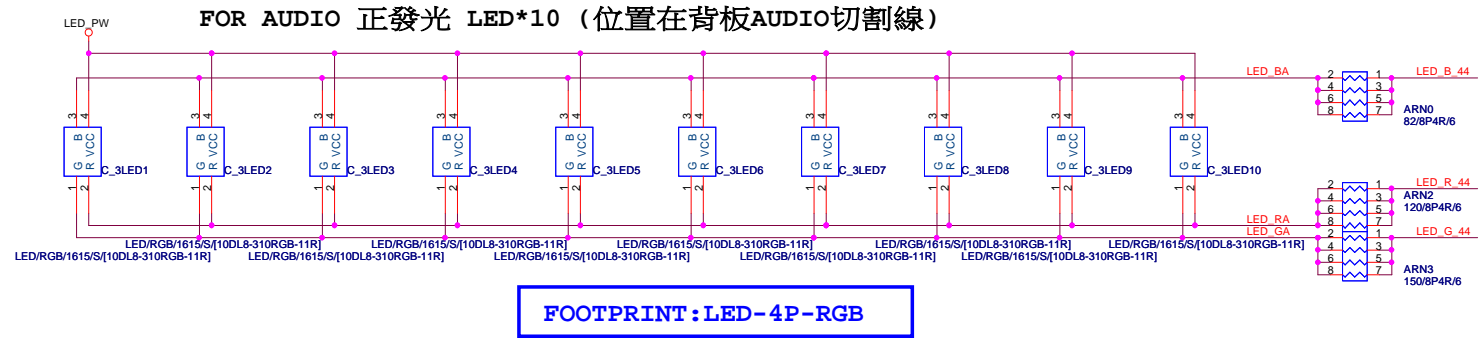
SMBUS

SMBUS

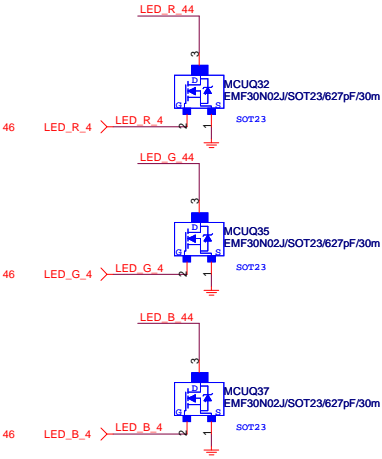
SMBUS

第三區 LED

第四區 LED



第四區 LED CONTROL

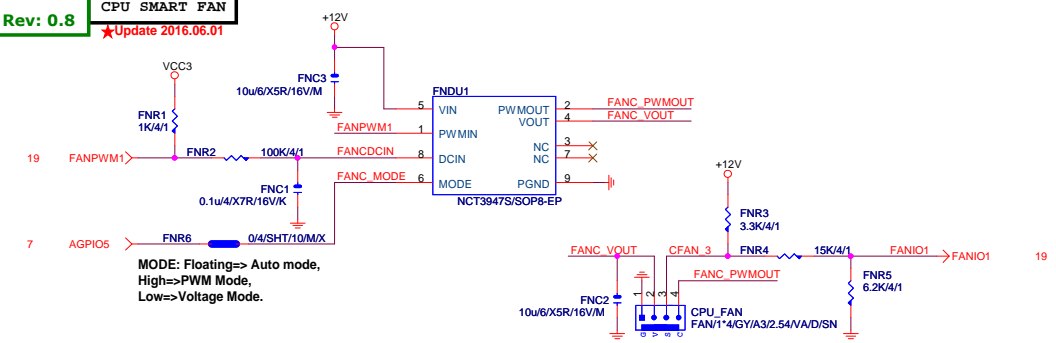


**GIGABYTE™**

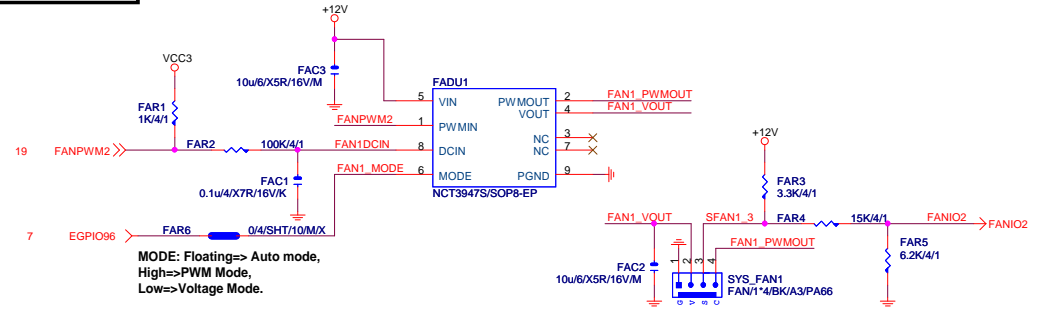
Title		
MODEL / PCB /AUDIO/PCIE LED		
Size	Document Number	Rev
Custom	X570 AORUS ELITE	1.0
Date:	Thursday, May 30, 2019	Sheet 47 of 55



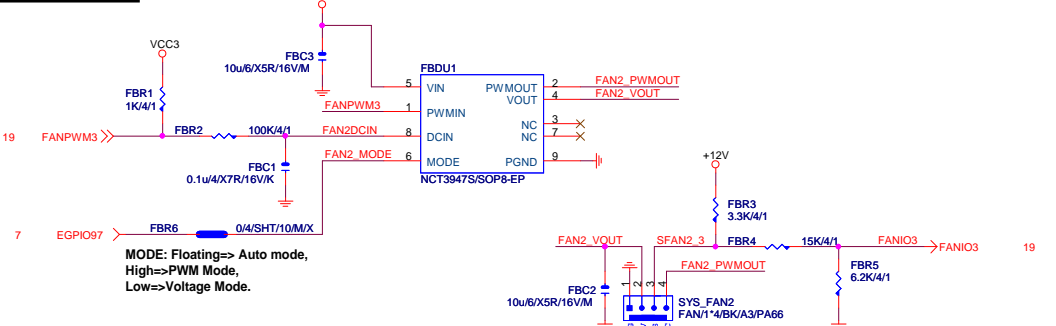




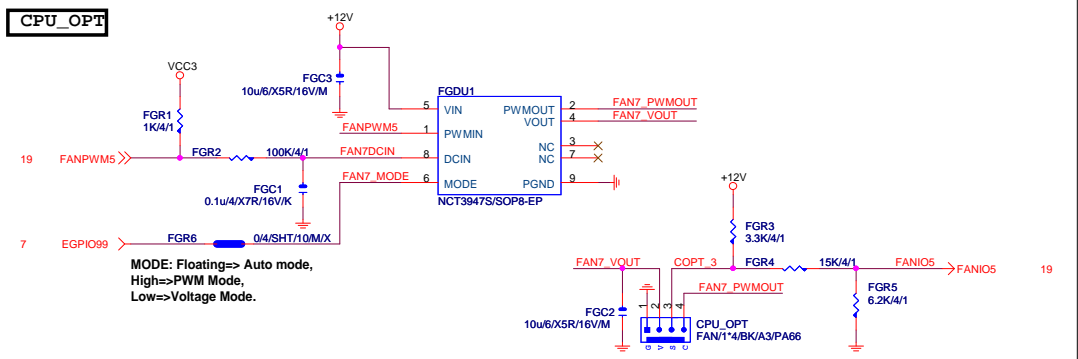
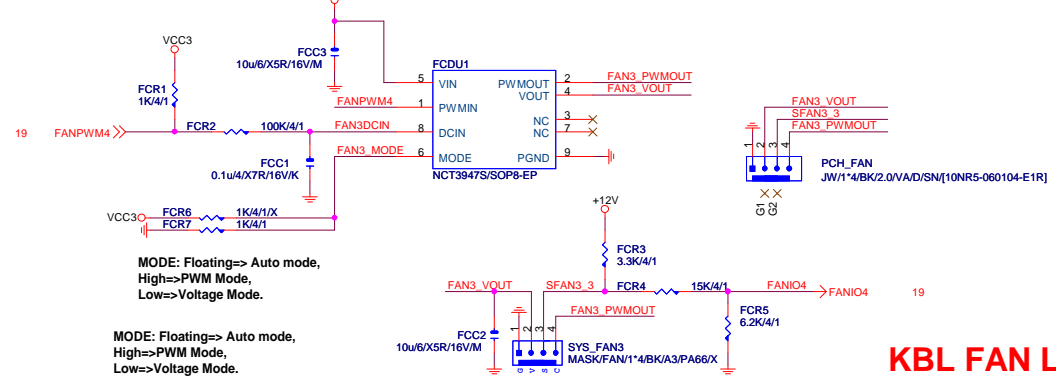
**SYSTEM FAN1**



**SYSTEM FAN2**



**SYSTEM FAN3**



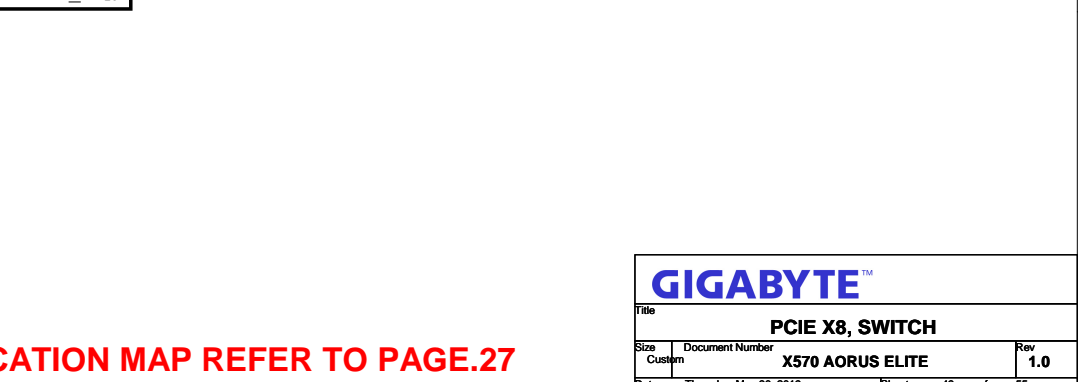
**SYSTEM FAN5 PUMP**



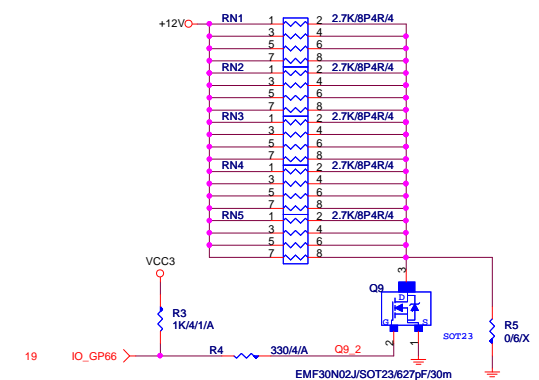
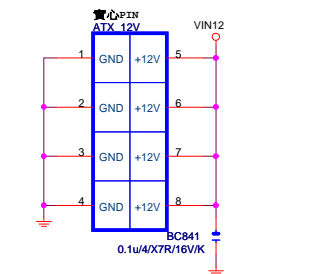
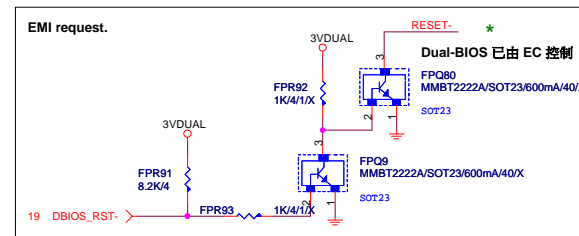
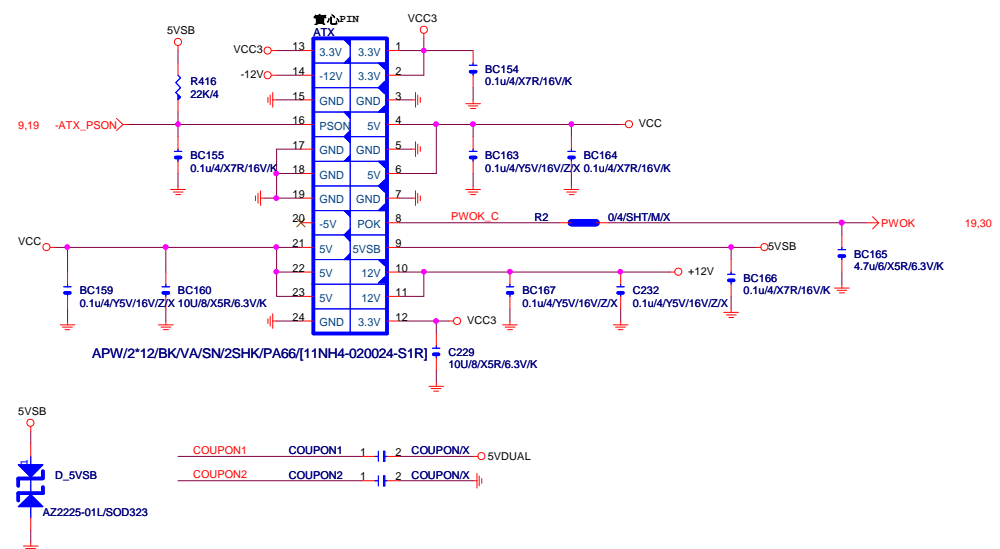
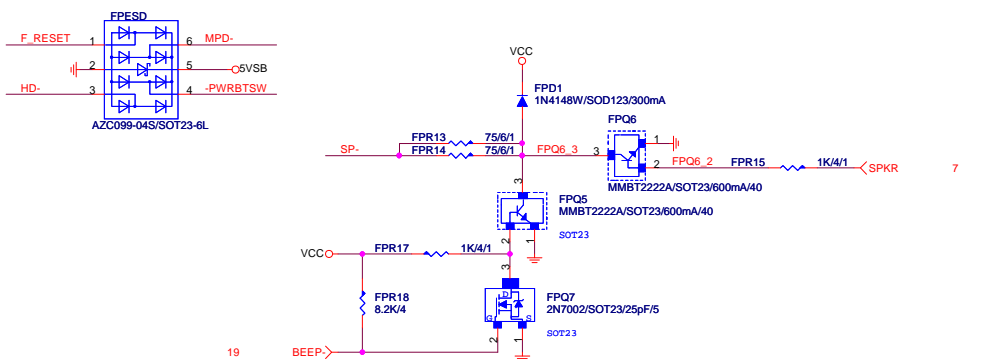
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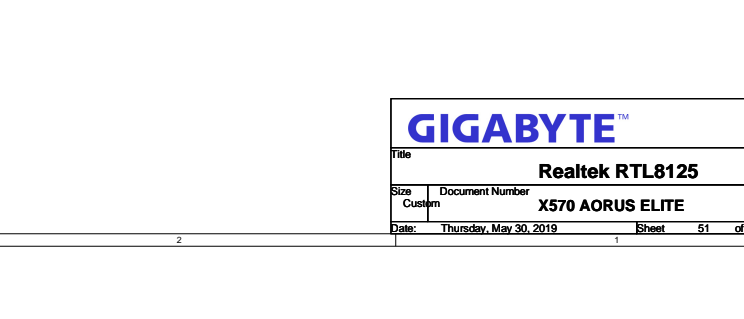
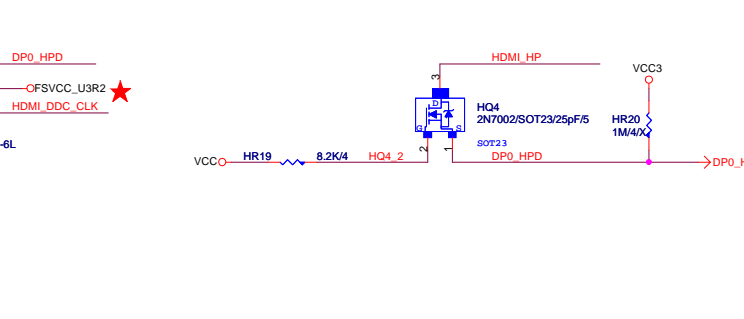
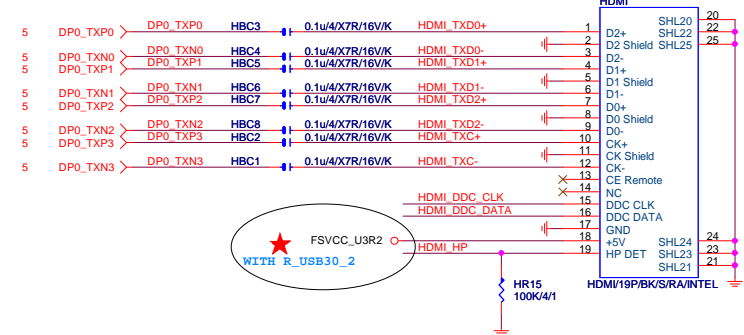
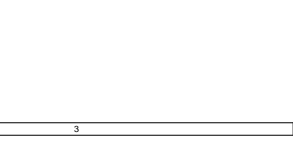
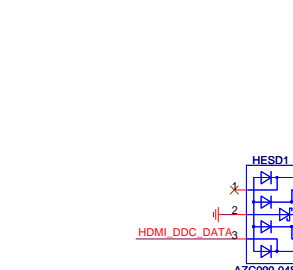
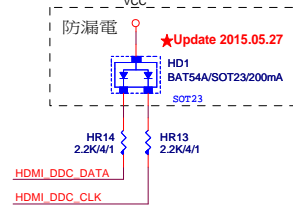
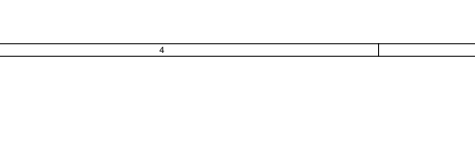
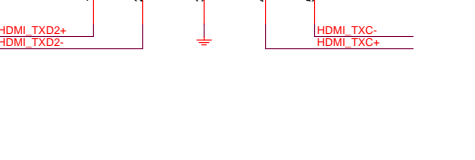
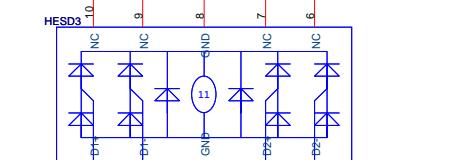
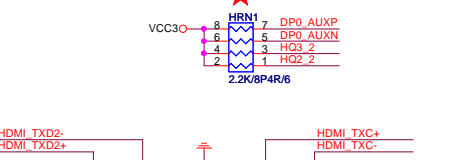
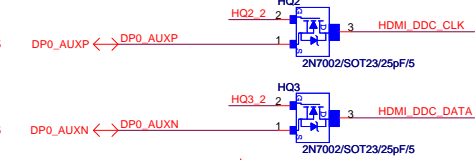
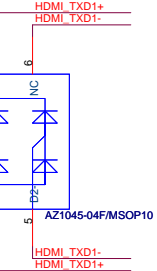
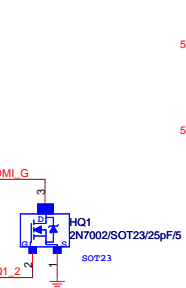
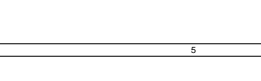
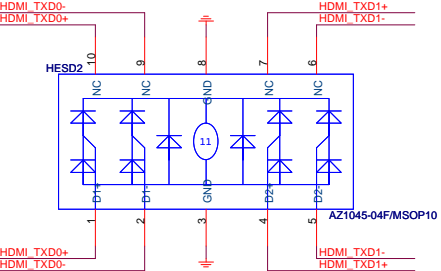
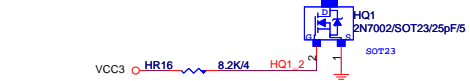
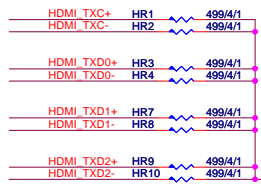


**SYSTEM\_FAN4**



**KBL FAN LOCATION MAP REFER TO PAGE.27**

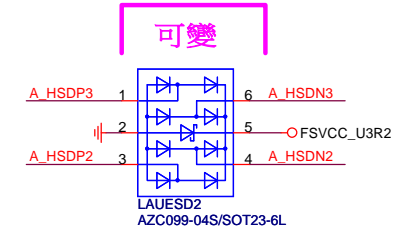




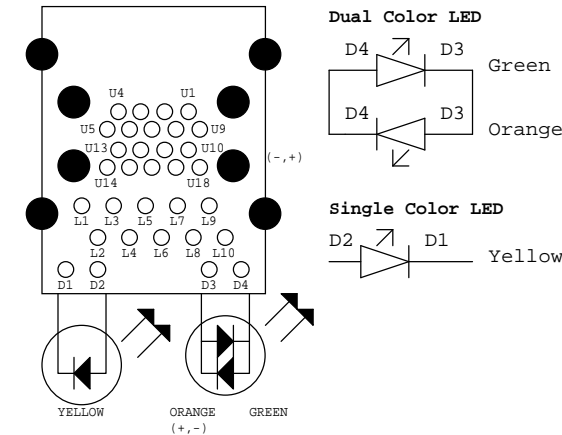
GIGABYTE™			
Title			
Realtek RTL8125			
Size	Document Number	Rev	
Custom	X570 AORUS ELITE	1.0	
Date:	Thursday, May 30, 2019	Sheet	51 of 55

USB\_LAN CONNECTOR R1.0

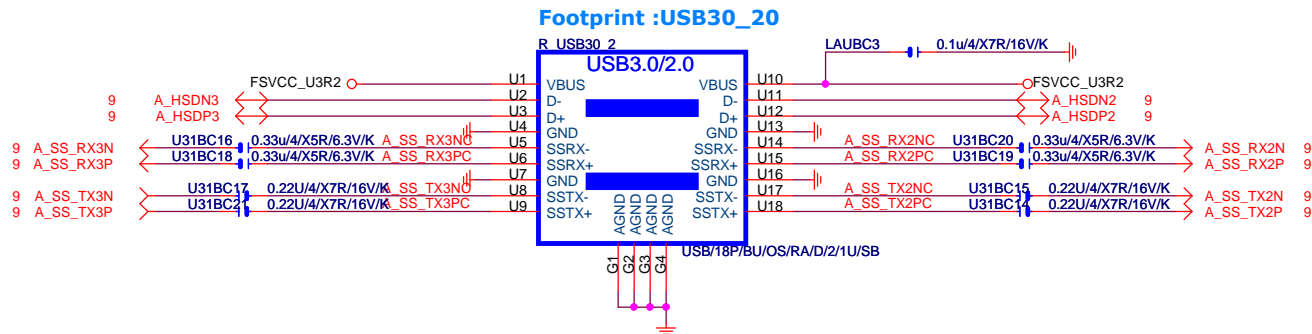
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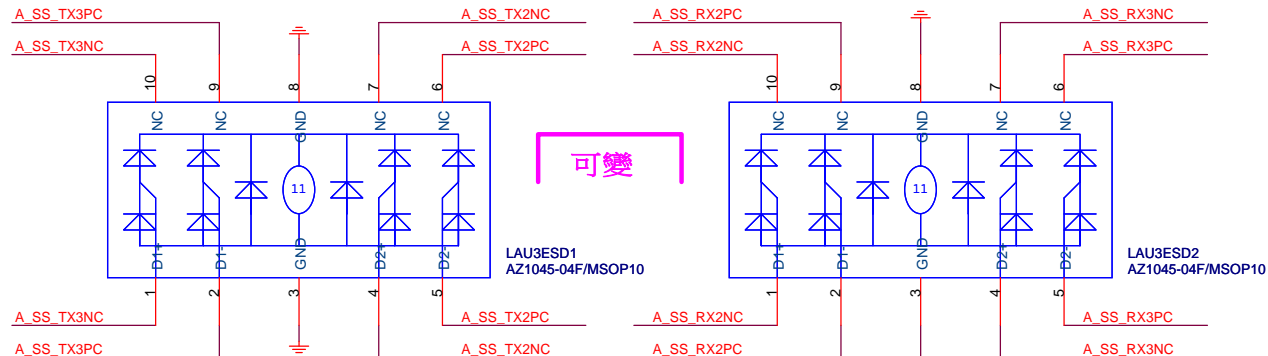
USB30\_LAN LAYOUT示意圖



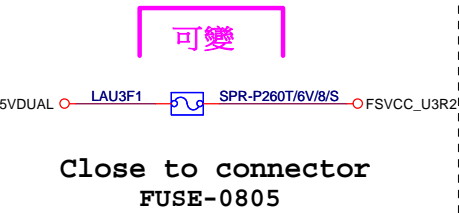
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RMA ESD PROTECT note:可變更USB\_NAME



USB POWER note:可變更FUSE



EMI SHORT PAD PS:視EMI需求

LAN POWER note:lan power連接及電流

**GIGABYTE™**

Title  
**Realtek RTL8125**

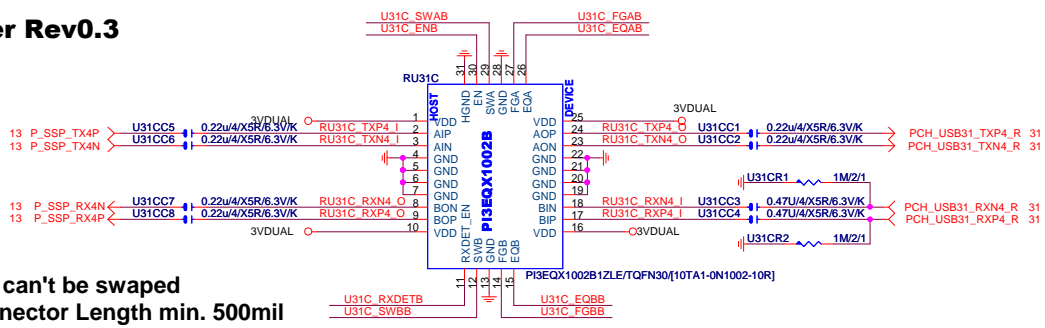
Size Document Number  
Custom **X570 AORUS ELITE**

Date: Thursday, May 30, 2019 Sheet 52 of 55

Rev **1.0**



TypeA Redriver Rev0.3



- Layout Rule:
1. Differential Pair can't be swaped
  2. Redriver to Connector Length min. 500mil

